

---

# HA13150A

21 W × 4-Channel BTL Power IC

# HITACHI

ADE-207-107  
1st. Edition

---

## Description

HA13150A is a four-channel BTL amplifier IC designed for car audio, featuring high output and low distortion, and applicable to digital audio equipment. It provides 21 W output per channel, with a 14.4 V power supply and at 10% distortion.

## Functions

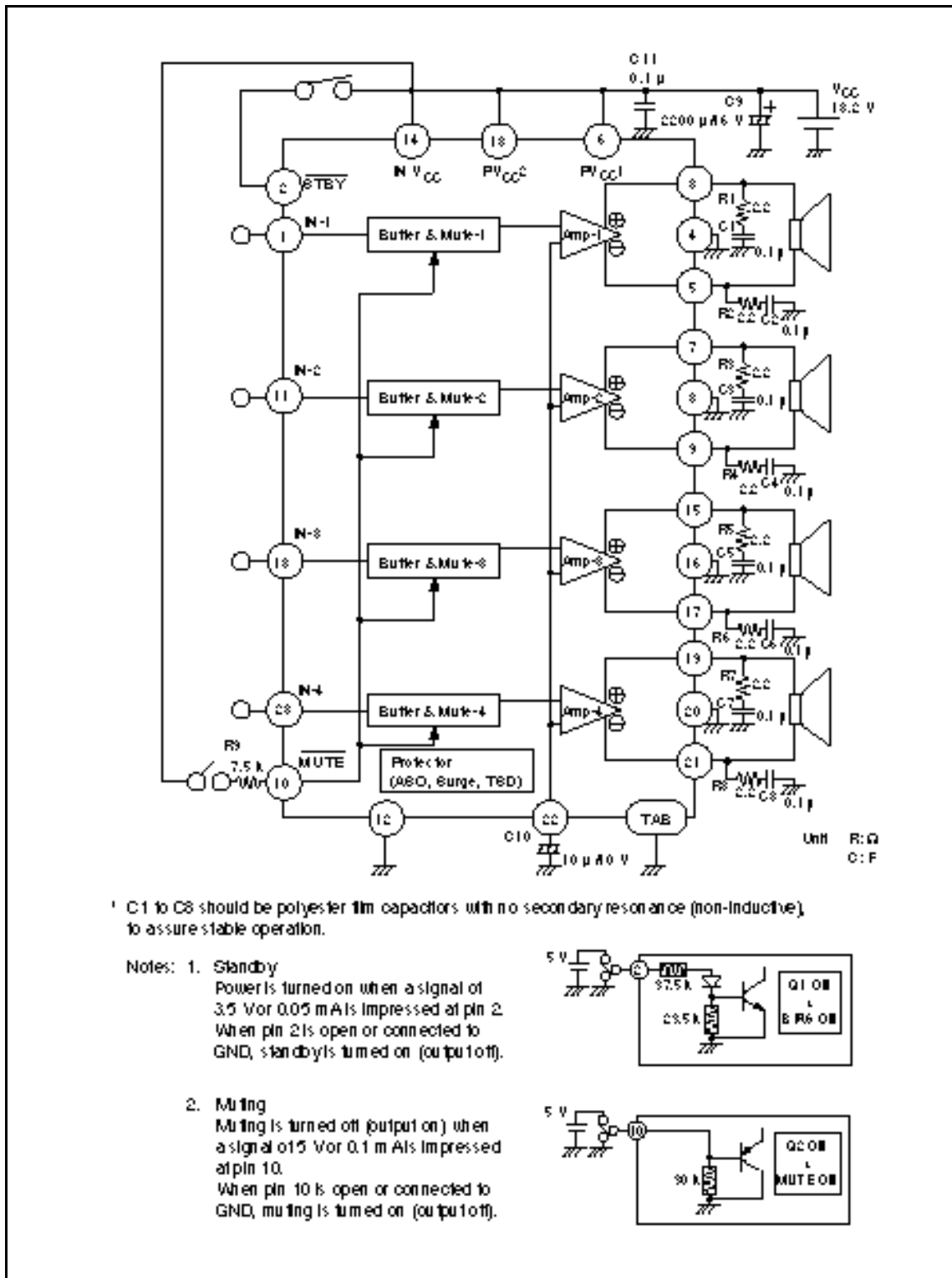
- Built-in standby circuit
- Built-in muting circuit
- Built-in protection circuits (surge, TSD, and ASO)

## Features

- Requires few external parts
- Low distortion (total harmonic distortion = 0.01% at 3 W)
- Low noise (at  $R_g = 620 \Omega$ , noise is 0.15 mV (muting off) or 0.1 mV (muting on))
- Popping noise minimized
- Highly reliable current-limiting ASO protector keeps speakers safe from all kinds of trouble. Reliability is further enhanced by a fast-acting thermal shutdown protection circuit with on/off hysteresis.

# HA13150A

## Block Diagram



## Absolute Maximum Ratings (Ta = 25°C)

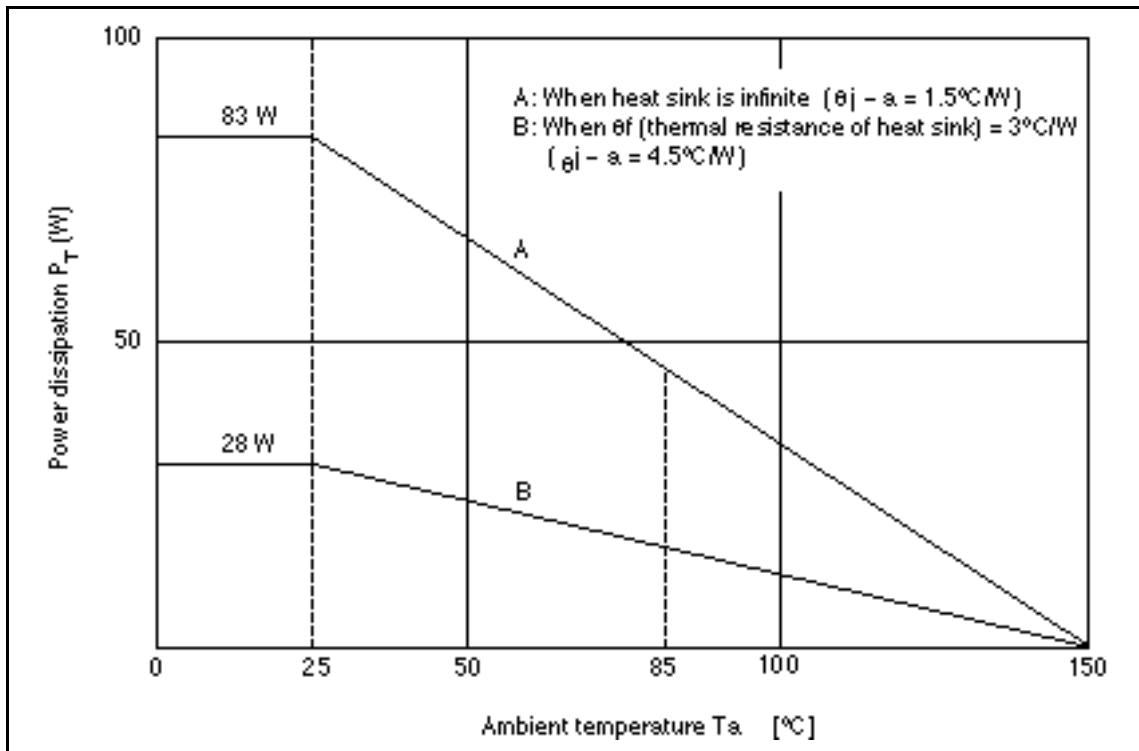
Item	Symbol	Rating	Unit	Remarks
------	--------	--------	------	---------

**HITACHI**

## HA13150A

Operating supply voltage	$V_{CC}$	18	V
Supply voltage when no signal * <sup>1</sup>	$V_{CC}$ (DC)	26	V
Peak supply voltage * <sup>2</sup>	$V_{CC}$ (PEAK)	50	V
Output current * <sup>3</sup>	$I_O$ (PEAK)	4	A
Power dissipation * <sup>4</sup>	$P_T$	83	W
Junction temperature	$T_j$	150	°C
Operating temperature	$T_{opr}$	-30 to +85	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

- Notes: 1. Tolerance within 30 seconds  
 2. Tolerance in surge pulse waveform  
 3. Value per 1 channel  
 4. Value when attached on the infinite heat sink plate at  $T_a = 25^\circ\text{C}$ .  
 The derating curve is as shown in the graph below.

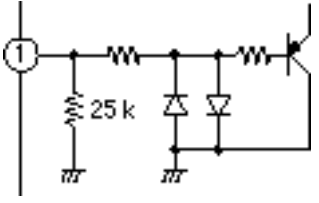
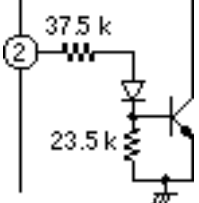
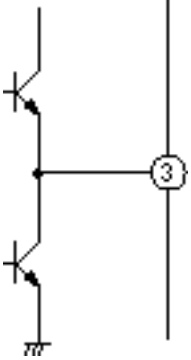
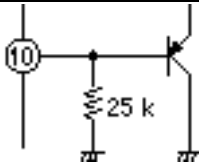


## HA13150A

**Electrical Characteristics** ( $V_{CC} = 13.2 \text{ V}$ ,  $f = 1 \text{ kHz}$ ,  $R_L = 4 \text{ } \Omega$ ,  $R_g = 620 \text{ } \Omega$ ,  $T_a = 25^\circ\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Current when no signal	I <sub>q1</sub>	—	240	—	mA	V <sub>in</sub> = 0
Output offset voltage	V <sub>q</sub>	-250	0	+250	mV	
Gain	G <sub>v</sub>	30.5	32	33.5	dB	
Gain difference between channels	G <sub>v</sub>	-1.5	0	+1.5	dB	
Rated output power	P <sub>o</sub>	—	18	—	W	V <sub>CC</sub> = 13.2 V R <sub>L</sub> = 4 $\Omega$ , THD = 10%
Max output power	P <sub>o</sub> max	—	30	—		V <sub>CC</sub> = 13.7 V R <sub>L</sub> = 4 $\Omega$ , THD = Max
Total harmonic distortion	T.H.D	—	0.01	—	%	P <sub>o</sub> = 3 W
Output noise voltage	W <sub>BN</sub>	—	0.15	0.5	mV <sub>rms</sub>	R <sub>g</sub> = 0 BW = 20 to 20 kHz
Ripple rejection	SVR	—	55	—	dB	R <sub>g</sub> = 600 f = 120 Hz
Channel crosstalk	C.T	—	70	—	dB	R <sub>g</sub> = 600 V <sub>out</sub> = 0 dBm
Input impedance	R <sub>in</sub>	—	25	—	k	
Standby current	I <sub>q2</sub>	—	—	200	$\mu\text{A}$	
Standby control voltage (high)	V <sub>STH</sub>	3.5	—	V <sub>CC</sub>	V	
Standby control voltage (low)	V <sub>STL</sub>	0	—	1.5	V	
Muting control voltage (high)	V <sub>MH</sub>	3.5	—	V <sub>CC</sub>	V	
Muting control voltage (low)	V <sub>ML</sub>	0	—	1.5	V	
Muting attenuation	A <sub>TTM</sub>	—	70	—	dB	V <sub>out</sub> = 0 dBm

**Pin Explanation**

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
1	IN1	CH1 INPUT	25 k (Typ)	0 V	
11	IN2	CH2 INPUT			
13	IN3	CH3 INPUT			
23	IN4	CH4 INPUT			
2	STBY	Standby control	90 k (at Trs. cutoff)	—	
3	OUT1 (+)	CH1 OUTPUT	—	$V_{cc}/2$	
5	OUT1 (-)				
7	OUT2 (+)	CH2 OUTPUT			
9	OUT2 (-)				
15	OUT3 (+)	CH3 OUTPUT			
17	OUT3 (-)				
19	OUT4 (+)	CH4 OUTPUT			
21	OUT4 (-)				
10	MUTE	Muting control	25 k (Typ)	—	

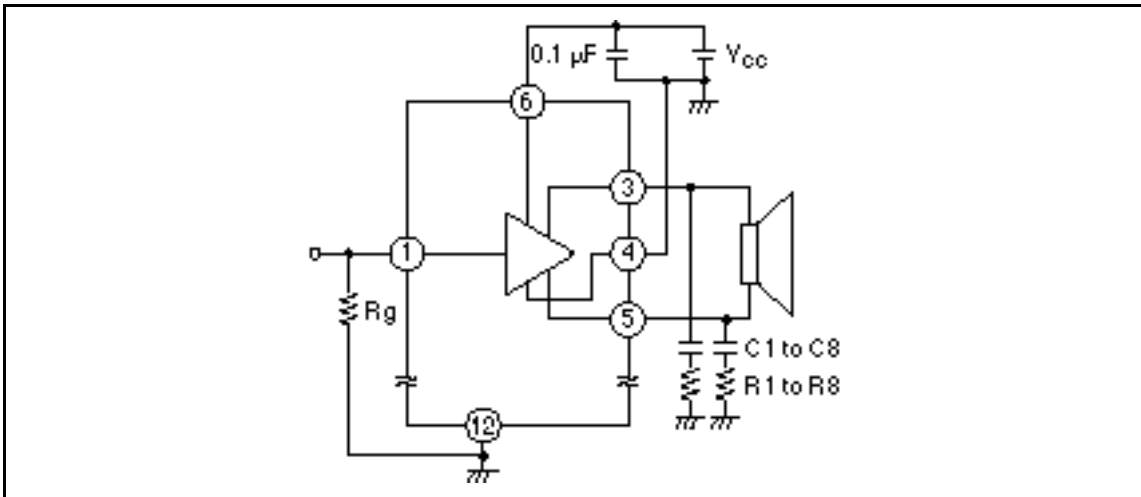
## HA13150A

### Pin Explanation (cont)

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
22	RIPPLE	Bias stability	—	$V_{CC}/2$	
6	$PV_{CC1}$	Power of output stage	—	$V_{CC}$	—
18	$PV_{CC2}$				
14	$INV_{CC}$	Power of input stage	—	$V_{CC}$	—
4	CH1 GND	CH1 power GND	—	—	—
8	CH2 GND	CH2 power GND			
16	CH3 GND	CH3 power GND			
20	CH4 GND	CH4 power GND			
12	IN GND	Input signal GND	—	—	—

### Point of Application Board Design

1. Notes on Application board's pattern design
  - For increasing stability, the connected line of  $V_{CC}$  and OUTGND is better to be made wider and lower impedance.
  - For increasing stability, it is better to place the capacitor between  $V_{CC}$  and GND ( $0.1 \mu\text{F}$ ) close to IC.
  - For increasing stability, it is better to place C1 to C8 and R1 to R8, which are for stopping oscillation, close to IC.
  - It is better to place the grounding of resistor ( $R_g$ ), between input line and ground, close to INGND (Pin 12) because if OUTGND is connected to the line between  $R_g$  and INGND, THD will become worse due to current from OUTGND.



**Figure 1** Notes on Application Board's Pattern Design

---

## HA13150A

---

### 2. How to reduce the popping noise by Muting circuit

At normal operating circuit, Muting circuit operates at high speed under 1  $\mu$ s.

In case popping noise becomes a problem, it is possible to reduce the popping noise by connecting capacitor, which determines the switching time constant, between pin 10 and GND. (Following figure 2)

We recommend value of capacitor greater than 1  $\mu$ F.

Also transitional popping noise can be reduced sharply by muting before  $V_{CC}$  and Standby are ON/OFF.

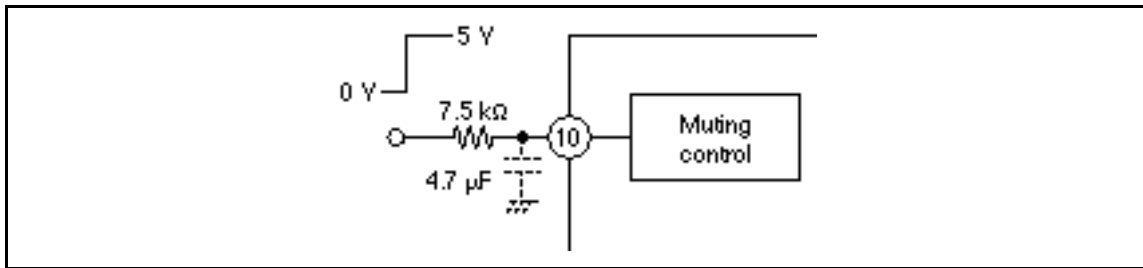
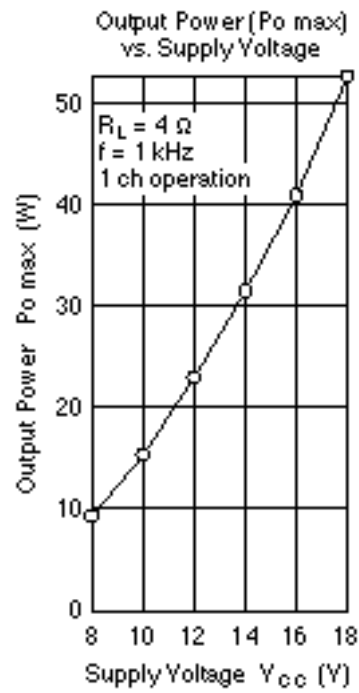
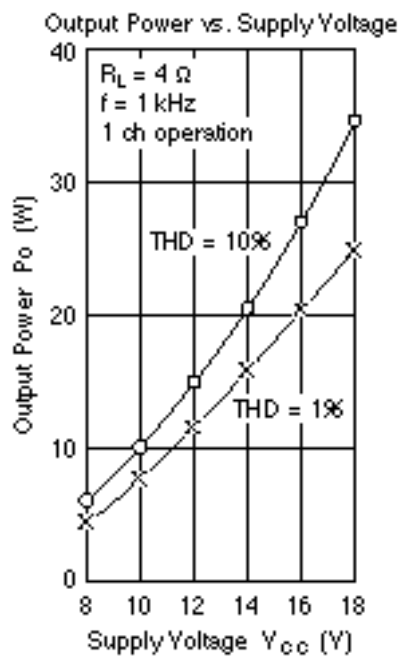
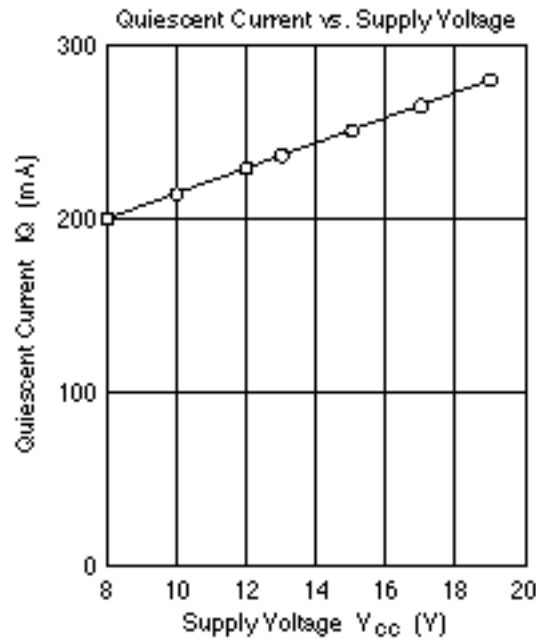


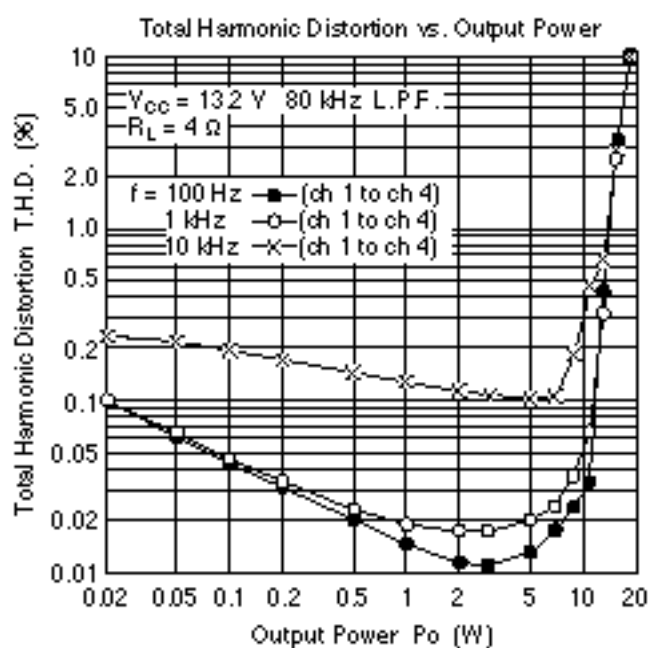
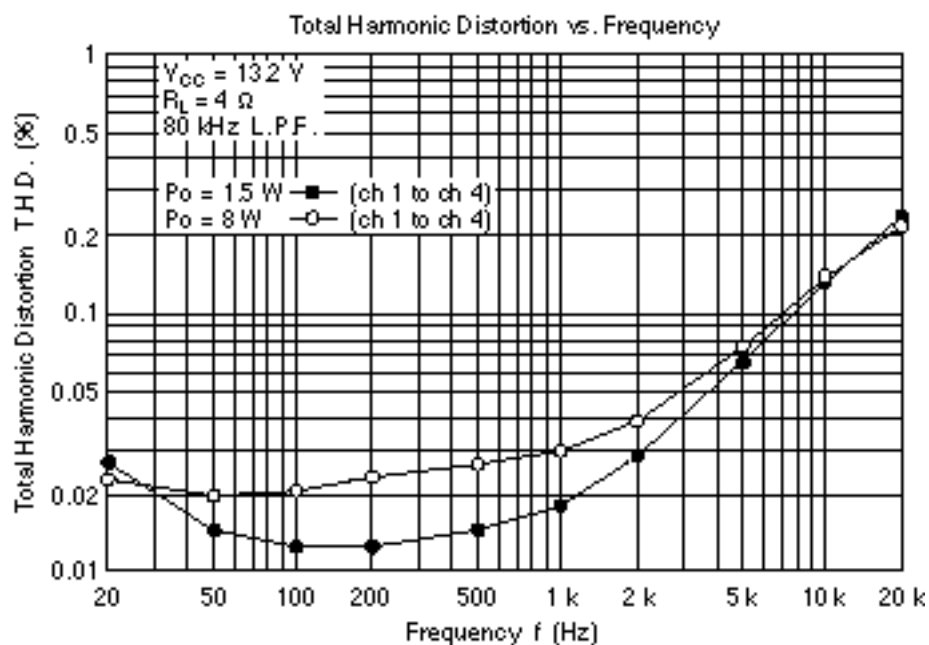
Figure 2 How to use Muting Circuit

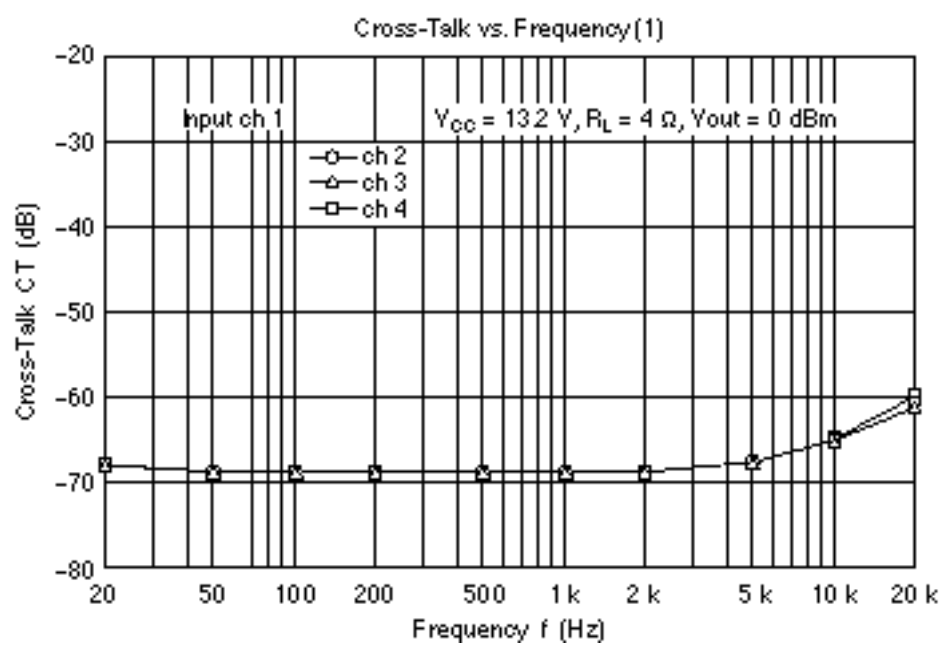
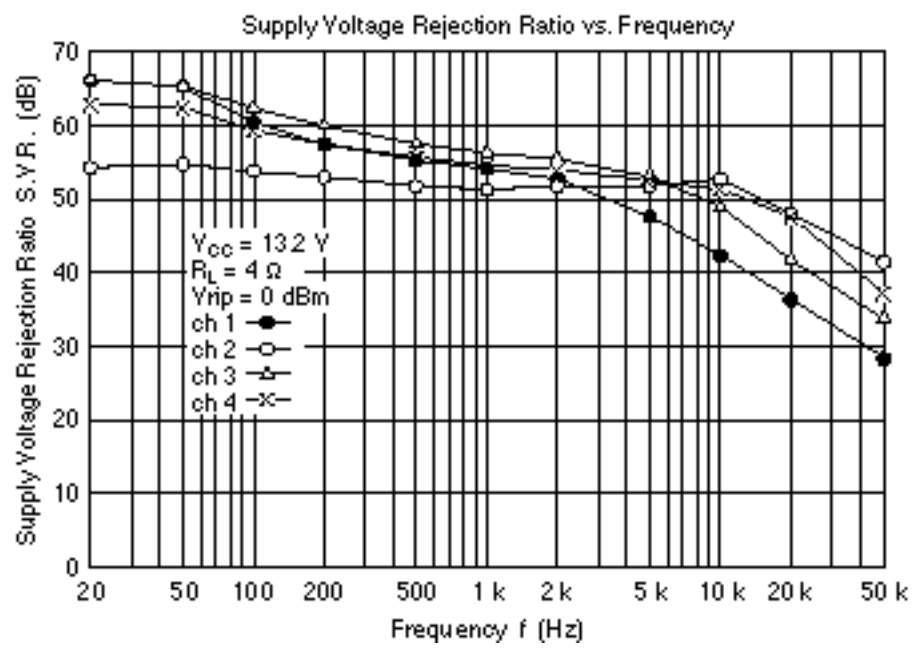
Table 1 Muting ON/OFF Time

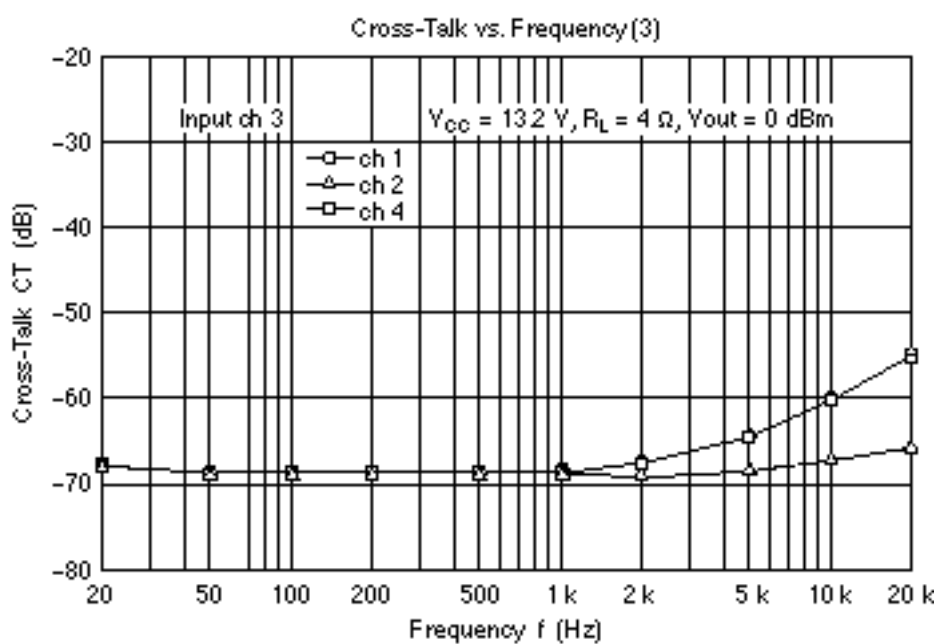
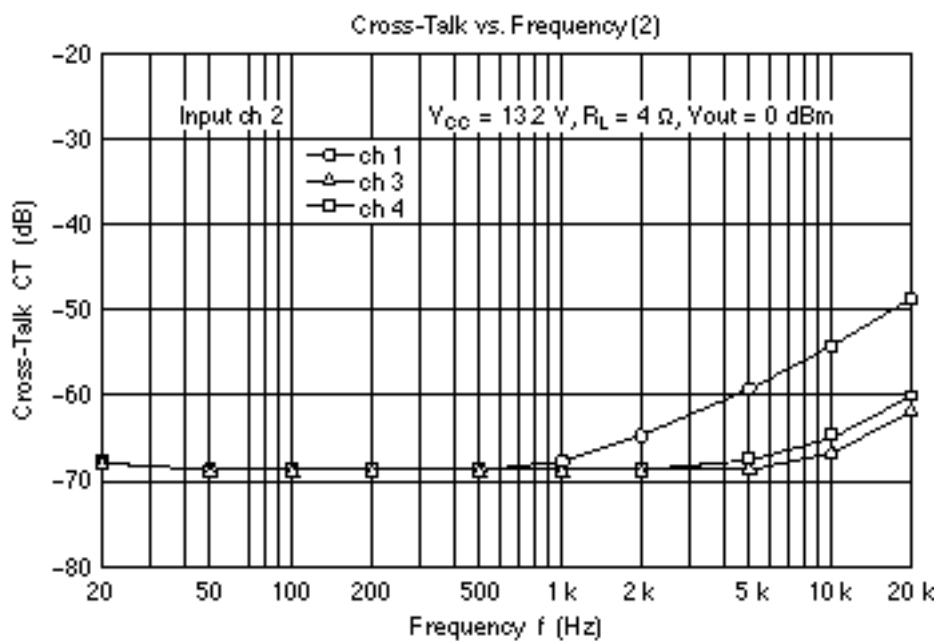
C ( $\mu$ F)	ON Time	OFF Time
nothing	under 1 $\mu$ s	under 1 $\mu$ s
0.47	2 ms	2 ms
4.7	19 ms	19 ms

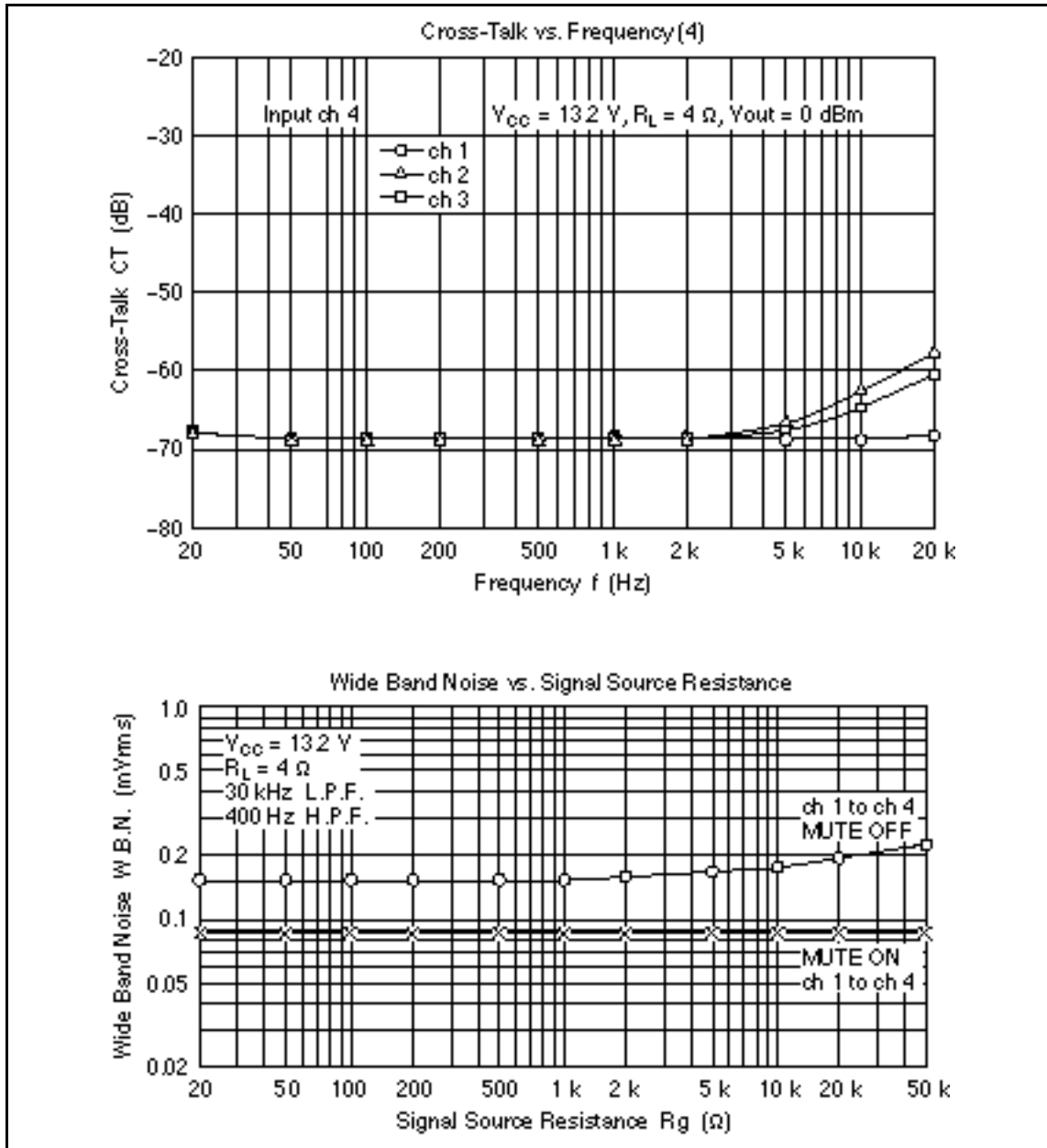




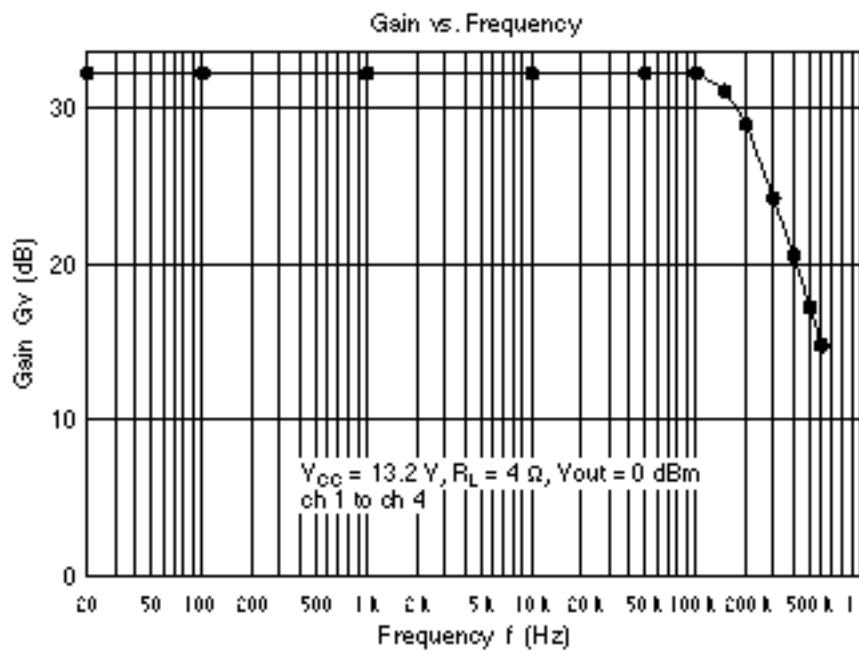
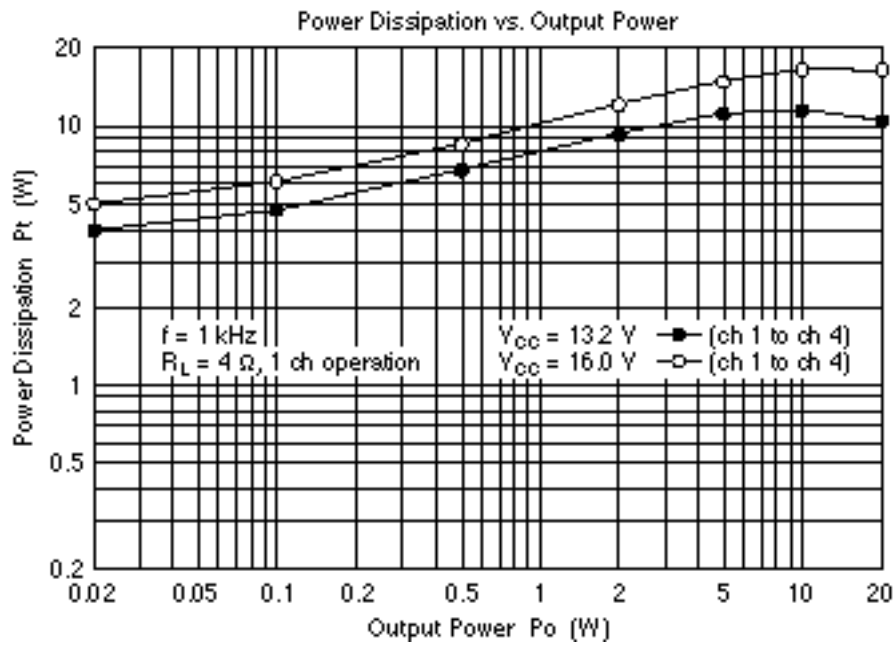








# HA13150A



**HITACHI**

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

---

---

# HITACHI

## **Hitachi, Ltd.**

Semiconductor & IC Div.

Nippon Bldg., 2-5-2, Ohite-machi, Chiyoda-ku, Tokyo 100, Japan

Tel Tokyo (03) 3270-2111

Fax (03) 3270-5109

For further information write to:

**Hitachi America, Ltd.**

Semiconductor & IC Div.

2000 Sierra Point Parkway

Folsom, CA 94005-4835

U.S.A.

Tel 415-589-8300

Fax 415-589-4207

**Hitachi Europe GmbH**

Electronic Components Group

Continental Europe

Darnecker Straße 3

D-85622 Feldkirchen

München

Tel 089-9 91 80-0

Fax 089-9 29 30 00

**Hitachi Europe Ltd.**

Electronic Components Div.

Northern Europe Headquarters

Whitebrook Park

Lower Cookham Road

High Wycombe

Berkshire SL6 6YA

United Kingdom

Tel 0628-885000

Fax 0628-778322

**Hitachi Asia Pte. Ltd.**

45 Collyer Quay #20-00

Hitachi Tower

Singapore 0104

Tel 535-2100

Fax 535-1533

**Hitachi Asia (Hong Kong) Ltd.**

Unit 705, North Tower,

World Finance Centre

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon

Hong Kong

Tel 27359218

Fax 27308074