National Semiconductor

June 1989

54LS256/DM74LS256
Dual 4-Bit Addressable Latch

General Description

The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input ($\overline{E}$) and an active LOW Clear input ($\overline{CL}$). Each latch has a Data input (D) and four outputs (Q0–Q3).

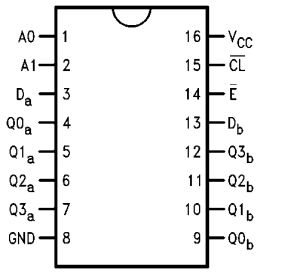
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q0–Q3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{CL}$ and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q0–Q3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{CL}$ = HIGH), changing more than one bit of the Address (A0, A1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{CL}$ = HIGH).

Features

- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Active low common clear

Connection Diagram

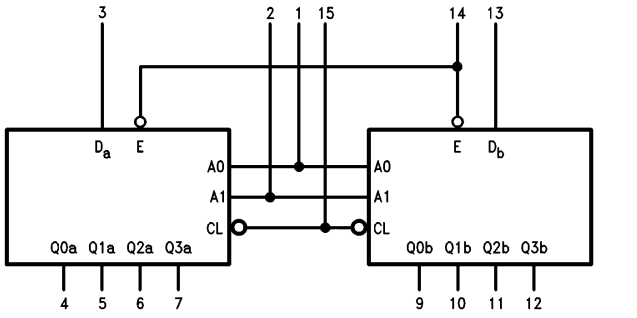
Dual-In-Line Package



TL/F/9823–1

Order Number 54LS256DMQB, 54LS256FMQB or DM74LS256N
See NS Package Number J16A, N16E or W16A

Logic Symbol



TL/F/9823–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0, A1	Common Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Common Enable Input (Active LOW)
$\overline{CL}$	Conditional Clear Input (Active LOW)
$Q0_a$–Q_3a	Side A Latch Outputs
$Q0_b$–Q_3b	Side B Latch Outputs

RRD-B30M115/Printed in U. S. A.

Truth Table

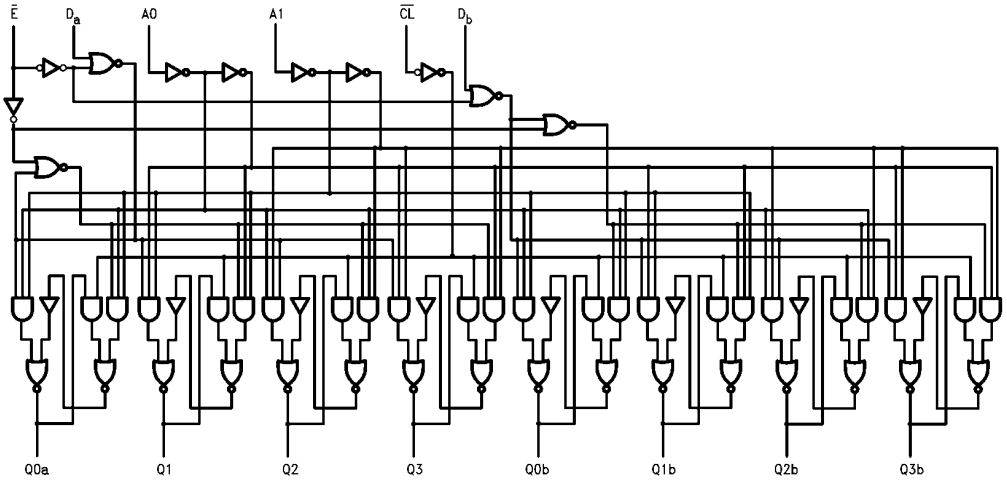
Inputs				Outputs				Mode
$\overline{CL}$	$\overline{E}$	A0	A1	Q0	Q1	Q2	Q3	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable
H	L	H	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	Latch
H	L	L	H	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	
H	L	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

$t-1$ = Bit time before address change or rising edge of E
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Mode Selection

$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

Logic Diagram



TL/F/9823–3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS256			DM74LS256			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}$	20			20			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}$	0			0			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}$	15			15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}$	0			0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, A_n to $\overline{E}$	0			0			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	17			17			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			0.1	mA
			$\overline{E}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{E}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs			−0.4	mA
			$\overline{E}$			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

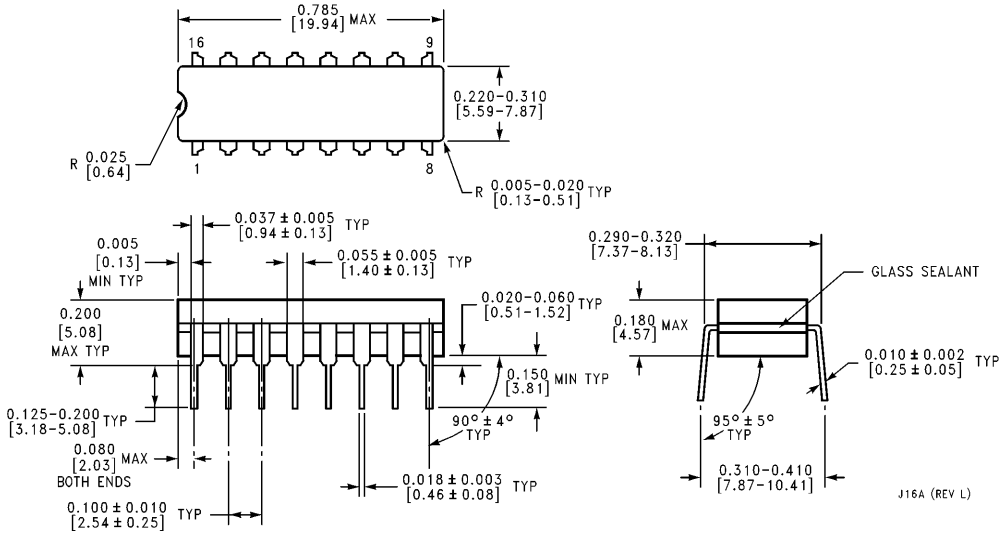
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

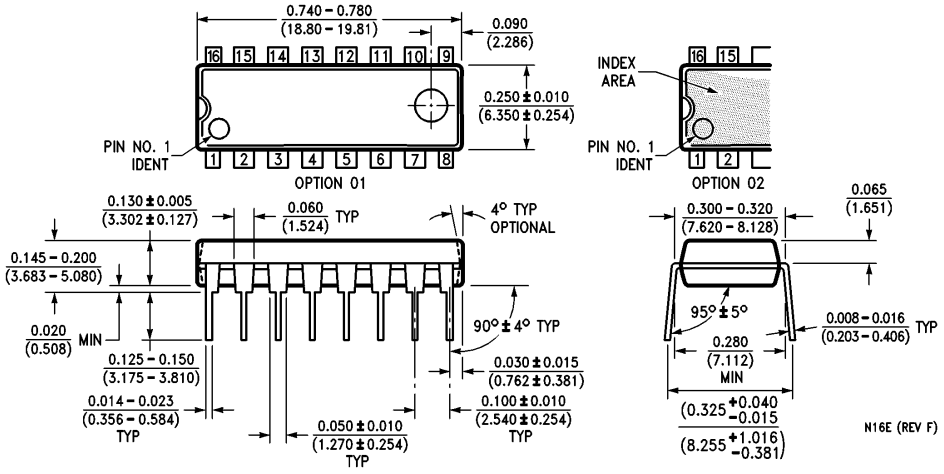
V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF	Units
		Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	27 24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	30 20	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	30 29	ns
t_{PLH}	Propagation Delay $\overline{CL}$ to Q_n	18	ns

Physical Dimensions inches (millimeters)

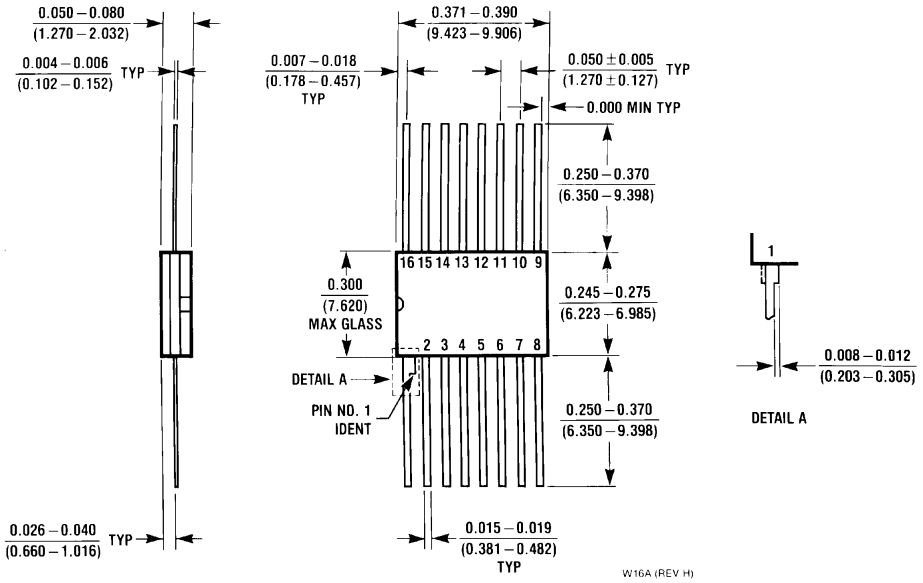


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS256DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS256N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS256FMQB
NS Package Number W16A

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