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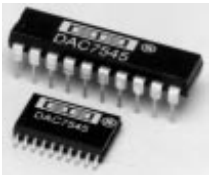


DAC7545

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

FEATURES

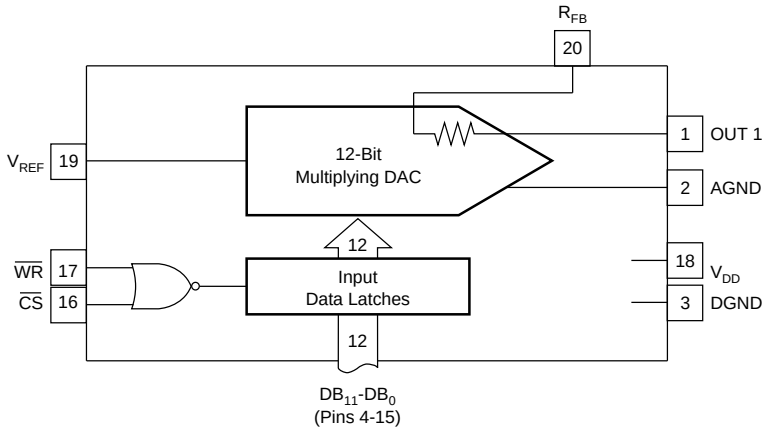
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2ppm/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- TTL/CMOS LOGIC COMPATIBLE
- LOW OUTPUT LEAKAGE: 10nA max
- LOW OUTPUT CAPACITANCE: 70pF max
- DIRECT REPLACEMENT FOR AD7545, PM-7545

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin plastic DIP or 20-lead plastic SOIC packages. Devices are specified over the commercial.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and V_{DD} = +5V.



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SPECIFICATIONS

ELECTRICAL

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM, unless otherwise specified.

PARAMETER	GRADE	DAC7545 V_{DD} = +5V T_A = +25°C	DAC7545 V_{DD} = +5V T_{MAX}-T_{MIN}(1)	DAC7545 V_{DD} = +15V T_A = +25°C	DAC7545 V_{DD} = +15V T_{MAX}-T_{MIN}(1)	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Accuracy	J	±2	±2	±2	±2	LSB	
	K	±1	±1	±1	±1	LSB	
	L	±1/2	±1/2	±1/2	±1/2	LSB	
	GL	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	J	±4	±4	±4	±4	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	K	±1	±1	±1	±1	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	L	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
	GL	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
Gain Error (with internal R_{FB})(2)	J	±20	±20	±25	±25	LSB	D/A register loaded with FFF_H. Gain error is adjustable using the circuits in Figures 2 and 3.
	K	±10	±10	±15	±15	LSB	
	L	±5	±6	±10	±10	LSB	
	GL	±1	±2	±6	±7	LSB	
Gain Temperature Coefficient(3) (ΔGain/ΔTemperature)	All	±5	±5	±10	±10	ppm/°C	Typical value is 2ppm/°C for V_{DD} = +5
DC Supply Rejection(3) (ΔGain/ΔV_{DD})	All	0.015	0.03	0.01	0.02	%/%	ΔV_{DD} ±5%
Output Leakage Current at Out 1	J, K, L, GL	10	50	10	50	nA	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
DYNAMIC PERFORMANCE							
Current Settling Time(3)	All	2	2	2	2	µs	To 1/2LSB. Out_1 Load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V
Propagation Delay(3) (from digital input change to 90% of final analog output)	All	300		250		ns	Out_1 Load = 100Ω. C_{EXT} = 13pF(4)
Glitch Energy	All	400		250		nV-s(5)	V_{REF} = ACOM
AC Feedback at I_{OUT} 1	All	5	5	5	5	mVp-p(5)	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT							
Input Resistance (pin 19 to AGND)	All	7 25	7 25	7 25	7 25	kΩ(6) kΩ	Input resistance TC = 300ppm/°C(5)
AC OUTPUTS							
Output Capacitance(3): $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	13.5	13.5	V(6)	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	1.5	1.5	V	
I_{IN} (Input Current)(7)	All	±1	±10	±1	±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance(3): DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V
SWITCHING CHARACTERISTICS(8)							
Chip Select to Write Setup Time, t_{CS}	All	280	380	180	200	ns(6)	See Timing Diagram
		200	270	120	150	ns(5)	
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns(6)	
Write Pulse Width, t_{WR}	All	250	400	160	240	ns(6)	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns(5)	
Data Setup Time, t_{DS}	All	140	210	90	120	ns(6)	
		100	150	60	80	ns(5)	
Data Hold Time, t_{DH}	All	10	10	10	10	ns(6)	
POWER SUPPLY, I_{DD}							
	All	2	2	2	2	mA	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	µA	All Digital Inputs 0V or V_{DD}
	All	10	10	10	10	µA(5)	All Digital Inputs 0V or V_{DD}

NOTES: (1) Temperature ranges—J, K, L, GL: 0°C to +70°C. (2) This includes the effect of 5ppm max, gain TC. (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical. (6) Minimum. (7) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (8) Sample tested at +25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS[1]

T_A = +25°C, unless otherwise noted.

V_{DD} to DGND	–0.3V, +17
Digital Input to DGND	–0.3V, V_{DD}
V_{RFB}, V_{REF}, to DGND	±25V
$V_{PIN\ 1}$ to DGND	–0.3V, V_{DD}
AGND to DGND	–0.3V, V_{DD}
Power Dissipation: Any Package to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature:	
Commercial J, K, L, GL	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

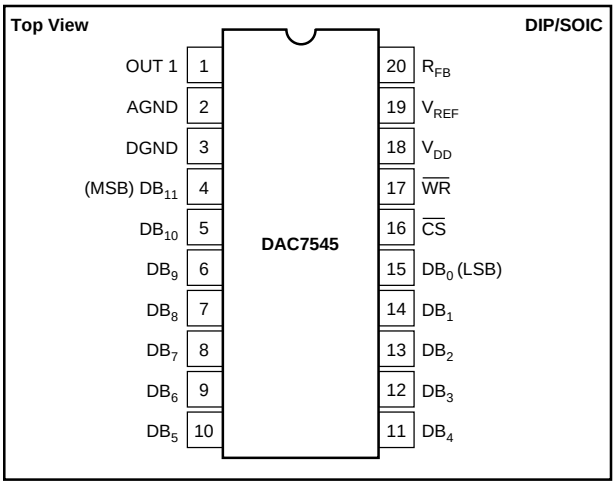
NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONNECTIONS



PACKAGE INFORMATION

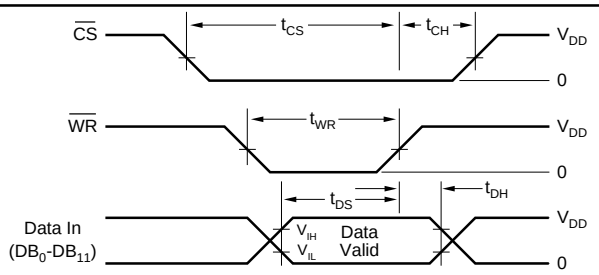
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7545JP	20-Pin PDIP	222
DAC7545KP	20-Pin PDIP	222
DAC7545LP	20-Pin PDIP	222
DAC7545GLP	20-Pin PDIP	222
DAC7545JU	20-Pin SOIC	221
DAC7545KU	20-Pin SOIC	221
DAC7545LU	20-Pin SOIC	221
DAC7545GLU	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

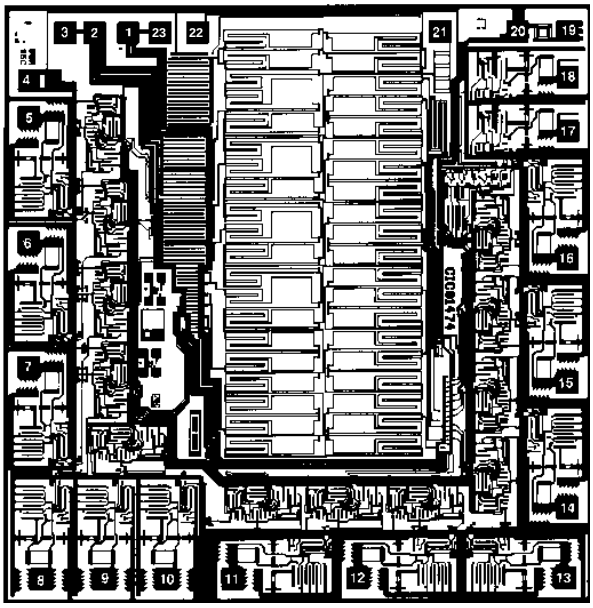
MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB) V_{DD} = +5V
DAC7545JP	Plastic DIP	0°C to +70°C	±2	±20
DAC7545KP	Plastic DIP	0°C to +70°C	±1	±10
DAC7545LP	Plastic DIP	0°C to +70°C	±1/2	±5
DAC7545GLP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7545JU	Plastic SOIC	0°C to +70°C	±2	±20
DAC7545KU	Plastic SOIC	0°C to +70°C	±1	±10
DAC7545LU	Plastic SOIC	0°C to +70°C	±1/2	±5
DAC7545GLU	Plastic SOIC	0°C to +70°C	±1/2	±1

WRITE CYCLE TIMING DIAGRAM



Mode Selection	
Write Mode	**Hold Mode**
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to Data Bus (DB_0-DB_{11}) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB_0-DB_{11}) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES: V_{DD} = +5V, t_R = t_F = 20ns. V_{DD} = +15V, t_R = t_F = 40ns. All inputs signal rise and fall times measured from 10% to 90% of V_{DD}. Timing measurement reference level is (V_{IH} + V_{IL})/2.



DAC7545 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	OUT 1	13	DB_3
2	AGND	14	DB_2
3	AGND	15	DB_1 (LSB)
4	DGND	16	DB_0
5	DB11	17	$\overline{CS}$
6	DB10	18	$\overline{WR}$
7	DB9	19	$\overline{XYR}$
8	DB8	20	V_{DD}
9	DB7	21	V_{REF}
10	DB6	22	R_{FB}
11	DB_5	23	OUT_1
12	DB_4		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	136 x 134 ±5	3.45 x 3.40 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7545 is –(4095/4096)(V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The current which appears at OUT 1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

The AC output error due to capacitive feedthrough from V_{REF} to OUT 1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time

The time required for the output to settle within ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-to-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND and an OPA600 as the output op amp and G_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7545 is guaranteed monotonic to 12 bits, except the J grade is specified to be 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of the digital-to-analog converter portion of the DAC7545. The current from the V_{REF} pin is switched from OUT 1 to AGND by the FET switch. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

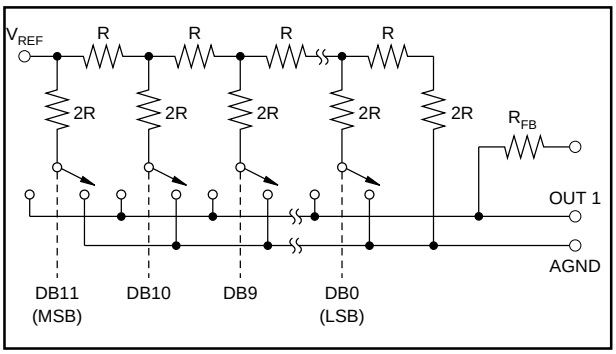


FIGURE 1. Simplified DAC Circuit of the DAC7545.

The output capacitance of the DAC7545 is code dependent and varies from a minimum value (70pF) at code 000H to a maximum (200pF) at code FFFH.

The input buffers are CMOS inverters, designed so that when the DAC7545 is operated from a 5V supply (V_{DD}), the logic threshold is TTL-compatible. Being simple CMOS inverters, there is a range of operation where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing this transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 2 shows the DAC7545 connected for unipolar operation. The high-grade DAC7545 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC7545JP, the gain error is specified to be ±25LSB. A range of adjustment of ±37LSB will be adequate. The equation below results in a value of 458Ω for the potentiometer (use 500Ω).

$$R_1 = \frac{R_{LADDER}}{4096} \text{ (3 x Gain Error)}$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 2 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 2.

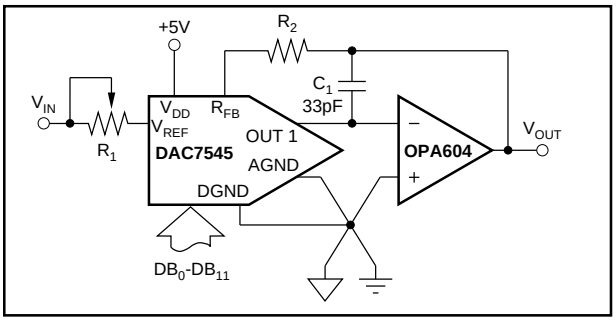


FIGURE 2. Unipolar Binary Operation.

BINARY CODE	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 V

TABLE I. Unipolar Codes.

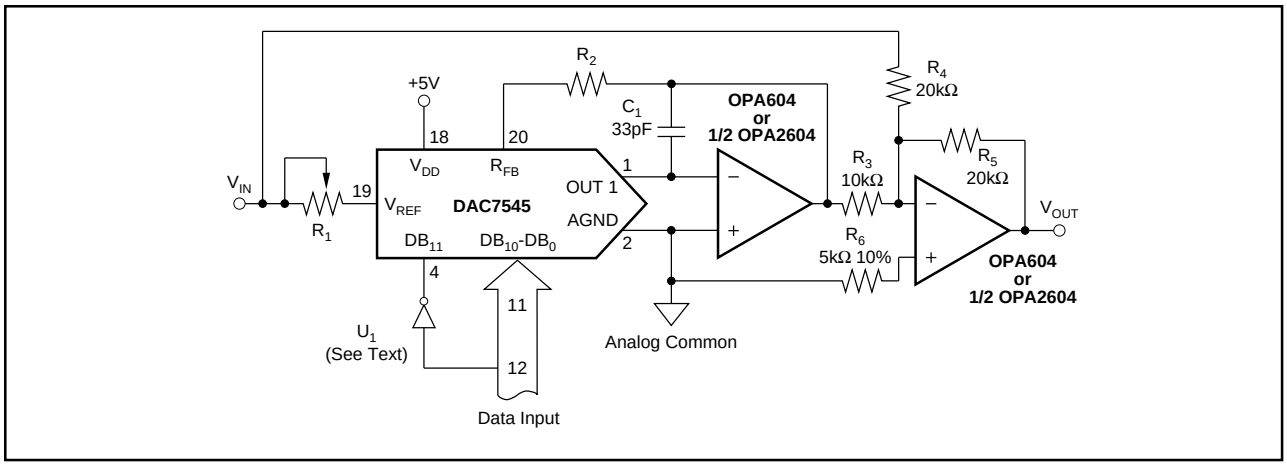


FIGURE 3. Bipolar Operation (Two's Complement Code).

BIPOLAR OPERATION

Figure 3 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter, U_1, on the MSB line converts two's complement input code to offset binary code. If the inversion is done in software, U_1 may be omitted.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

DATA INPUT	ANALOG OUTPUT
MSB LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 V
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

TABLE II. Two's Complement Code Table for Circuit of Figure 3.

DIGITALLY CONTROLLED GAIN BLOCK

Figure 4 shows a circuit for digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC7545. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback, and a saturated op amp output.

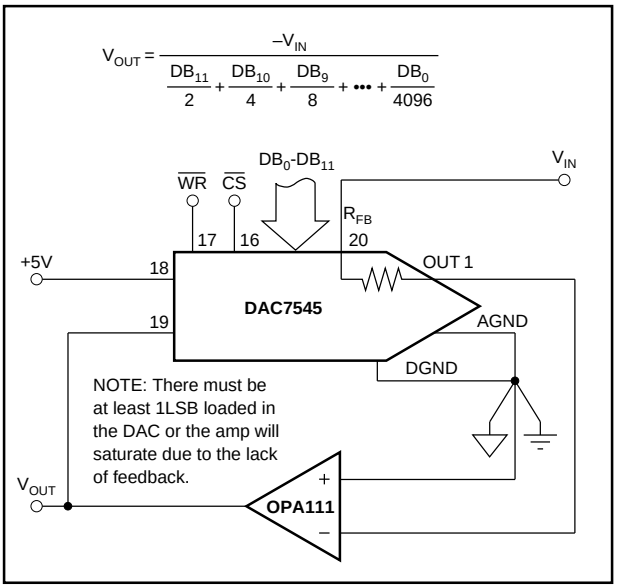


FIGURE 4. Digitally Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACs, such as the DAC7545, exhibit a code-dependent out resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage, V_{OS}, of the amplifier. Thus linearity depends upon the potential of OUT 1 and AGND being exactly equal to each other. Usually the DAC is connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than $(25 \times 10^{-6})(V_{REF})$ over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA627 for fixed reference applications and low bandwidth requirement. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA604 or 1/2 OPA2604 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise form triggering the high impedance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING TO MICROPROCESSORS

The DAC7545 can be directly interfaced to either an 8- or 16-bit microprocessor through its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ controls.

An 8-bit processor interface is shown in Figure 5. It uses two memory addresses, one for the lower 8 bits and one for the upper 4 bits of data into the DAC via the latch.

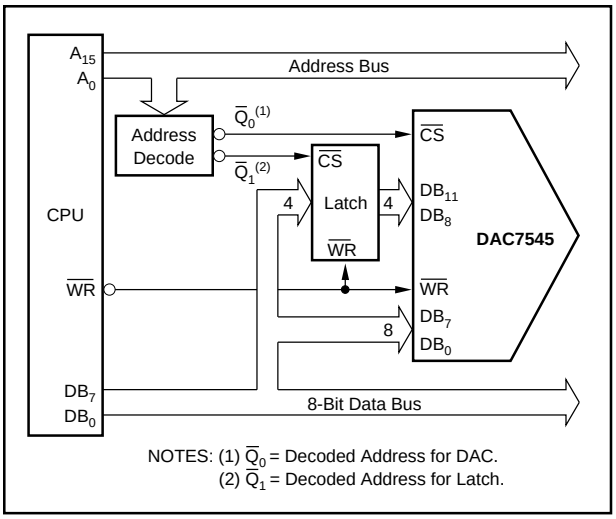
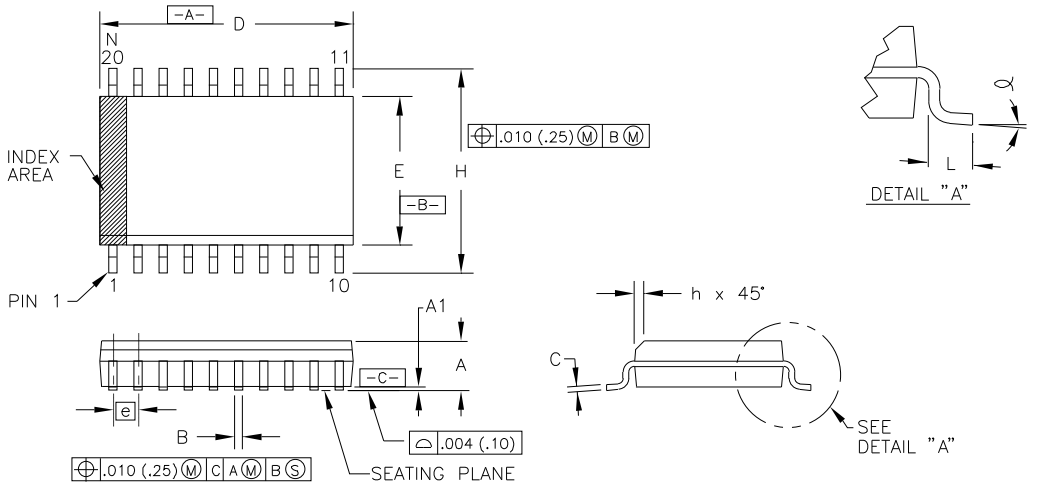


FIGURE 5. 8-Bit Processor Interface.

PACKAGE DRAWINGS

Package Number 221 - 20-LEAD SOIC

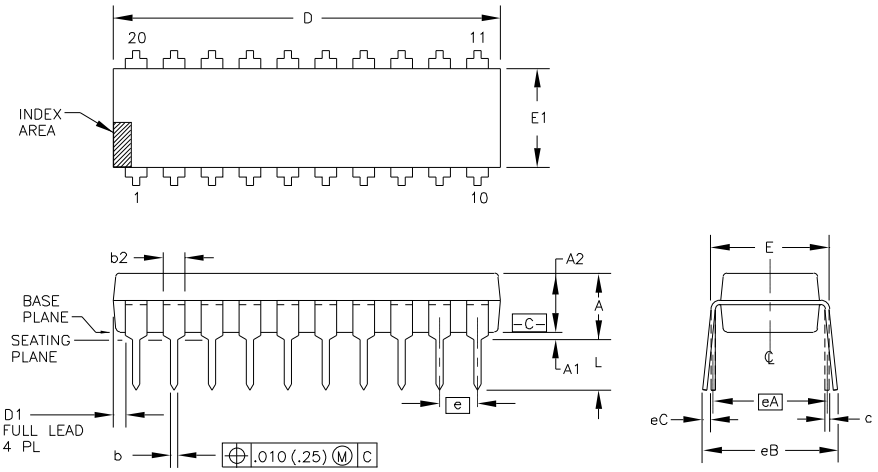


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.4961	.5118	12.60	13.00	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	20		20		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ221	REV.: C
JEDEC NUMBER: MS–013–AC	

Package Number 222 - 20-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	––	.210	––	5.33	3
A1	.015	––	0.38	––	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.980	1.060	24.89	26.92	4
D1	.005	––	0.13	––	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	––	.430	––	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	20		20		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ222	REV.: C
JEDEC NUMBER: MS–001–AD	