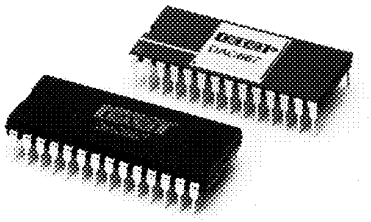
BURR - BROWN®



DAC667

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

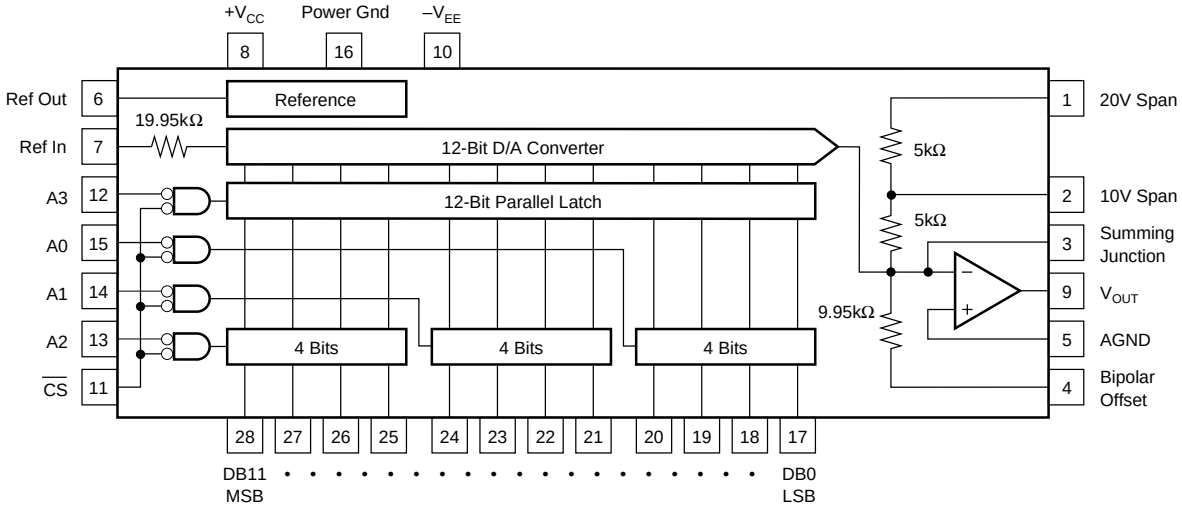
- ±1/2LSB MAX NONLINEARITY OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- MICROCOMPUTER INTERFACE: Double-Buffered Latch
- VOLTAGE OUTPUT: ±10V, ±5V, +10V With ±12V to ±15V Supplies
- LOW POWER DISSIPATION: 345mW typ
- PIN COMPATIBLE WITH AD667

DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microprocessor-compatible 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing to 4-, 8-, 12-, or 16-bit data buses. The input buffer latch holds the 12-bit data until it is transferred to an internal 12-bit D/A converter latch, giving precise timing control over an analog output change.

The DAC667 is specified to ±1/4LSB maximum linearity error (B and K grades) at +25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range. The DAC667 is available in two performance grades and in 28-pin, 0.6" wide plastic and ceramic DIP package types.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1091B Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667JP MIN	DAC667JP TYP	DAC667JP MAX	DAC667KP MIN	DAC667KP TYP	DAC667KP MAX	UNITS
DIGITAL INPUTS							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	0		+0.8	*		*	V
I_{IH} (VI_H = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load, C_F = 0)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = –11.4 to –16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
–11.4 to –16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	–40		+85	*		*	°C
Storage	–65		+125	*		*	°C

* Same as specification for DAC667JP.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground ..... 0V to +18V
V_{EE} to Power Ground ..... 0V to –18V
Digital Inputs (Pins 11–15, 17–28) to Power Ground ..... –1V to +7V
Ref In to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span Resistor to Reference Ground ..... ±12V
20V Span Resistor to Reference Ground ..... ±24V
Ref Out, V_{OUT} (Pins 6, 9) ..... Indefinite Short to Power Ground, Momentary Short To V_{CC}
Power Dissipation 1000mW

TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

All models, T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V.

ELECTRICAL (CONT)

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667AH MIN	DAC667AH TYP	DAC667AH MAX	DAC667BH MIN	DAC667BH TYP	DAC667BH MAX	UNITS
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})(1)							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	+0		+0.8	*		*	V
I_{IH} (V_{IH} = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error(2)		±0.1	±0.2		*	*	% of FSR(3)
Unipolar Offset Error(2)		±1	±2		*	*	LSB
Bipolar Zero(2)		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges(4)		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = –11.4 to –16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range(4)	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
–11.4 to –16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Operating	–40		+85	*		*	°C
Storage	–65		+150	*		*	°C

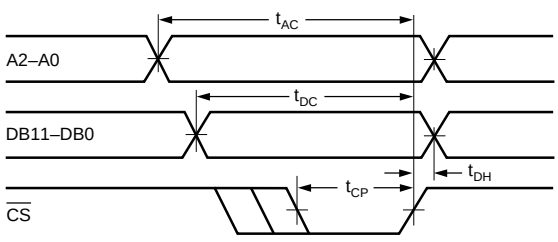
* Same as specification for DAC667AH.

NOTES: (1) The digital input specifications are 100% tested at +25°C and over the full temperature range. (2) Adjustable to zero. (3) FSR means full scale range and is 20V for ±10V range and 10V for the ±5V range. (4) ±10V full scale output can be achieved using ±11.4 supplies.

TIMING DIAGRAMS

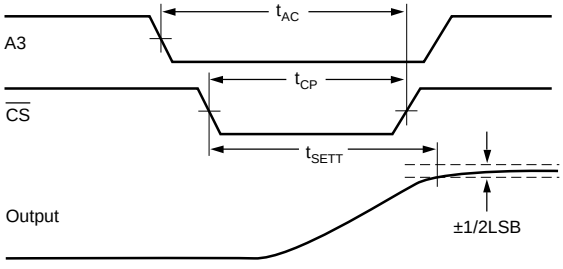
Write Cycle #1

Load first rank from Data Bus; A3 = 1.



Write Cycle #2

Load second rank from first rank; A2, A1, A0 = 1.



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC667JP	28-Pin Plastic DIP	215
DAC667KP	28-Pin Plastic DIP	215
DAC667AH	28LD Side-Brazed Ceramic DIP	149
DAC667BH	28LD Side-Brazed Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, max at 25°C	GAIN TC, max (ppm/°C)
DAC667JP	Plastic DIP	0 to +70	±1/2LSB	±30
DAC667KP	Plastic DIP	0 to +70	±1/4LSB	±15
DAC667AH	Ceramic DIP	–25 to +85	±1/2LSB	±30
DAC667BH	Ceramic DIP	–25 to +85	±1/4LSB	±15

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all ones and all zeros). DAC667 linearity error is specified at ±1/4LSB max at +25°C for B and K grades, and ±1/2LSB max for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. All grades of the DAC667 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Gain drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar offset drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar offset drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

Bipolar zero drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar zero drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for FSR output changes of 20V (10kΩ feedback) and 10V (5kΩ feedback), and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

OPERATION

DAC667 is a monolithic integrated-circuit 12-bit D/A converter. It is complete with 12-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface as shown in the front-page diagram.

INTERFACE LOGIC

The bus interface logic of the DAC667 consists of four independently addressable latches in two ranks. The first rank consists of three four-bit input latches which can be loaded directly from a 4-, 8-, 12- or 16-bit microprocessor/microcontroller bus. These latches hold data temporarily while a complete 12-bit word is assembled before loading it into the second rank of latches. This double buffered organization prevents the generation of spurious analog output values while the complete word is being assembled.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When the control signals return to logic 1, the data is latched. A truth table for the control signals is presented in Table I.

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable Four LSBs of First Rank
0	1	1	0	1	Enable Four Middle Bits of First Rank
0	1	0	1	1	Enable Four MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent
X = Don't care.					

TABLE I. DAC667 Truth Table.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the timing specifications on page 2 are met.

LOGIC INPUT COMPATIBILITY

The DAC667 digital inputs are TTL compatible (1.4V switching level) with a low leakage, high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

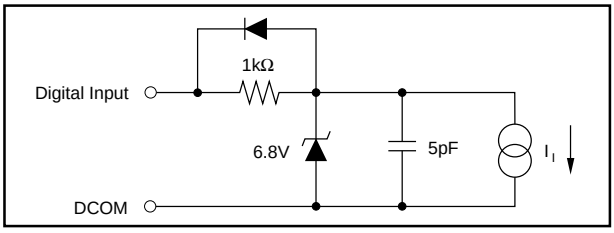


FIGURE 1. Equivalent Digital Input Circuit.

DAC667 data inputs will float to logic 1 and control inputs will float to logic 0 if left open. It is recommended that any unused inputs be connected to power common to improve noise immunity.

INPUT CODING

The DAC667 accepts positive-true binary input codes.

Input coding for unipolar analog output is straight binary (USB), where all zeros (000_{HEX}) on the data inputs gives a zero analog output and all ones (FFF_{HEX}) gives an analog output 1LSB below full scale.

Input coding for bipolar analog outputs is bipolar offset binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

The DAC667 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC667 contains a +10V reference which is trimmed to typically ±0.2% and tested and guaranteed to ±1%. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 50Ω. A trim potentiometer with a nominal value of 100Ω can be used to provide adjustment to zero gain error. If an external 10.000V reference is used, it may be necessary to increase the trim range slightly.

The reference output may be used to drive external loads, sourcing up to 5mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the converter will vary.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. The DAC667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range, a CMOS multiplying D/A is a better choice.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of offset and gain adjustments to a unipolar- and a bipolar-connected DAC667. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For unipolar (USB) operation, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) operation, apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. See Table II for calibration values and codes.

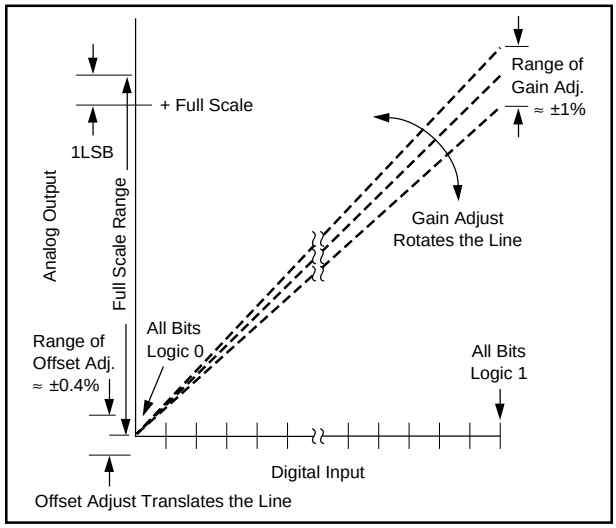


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

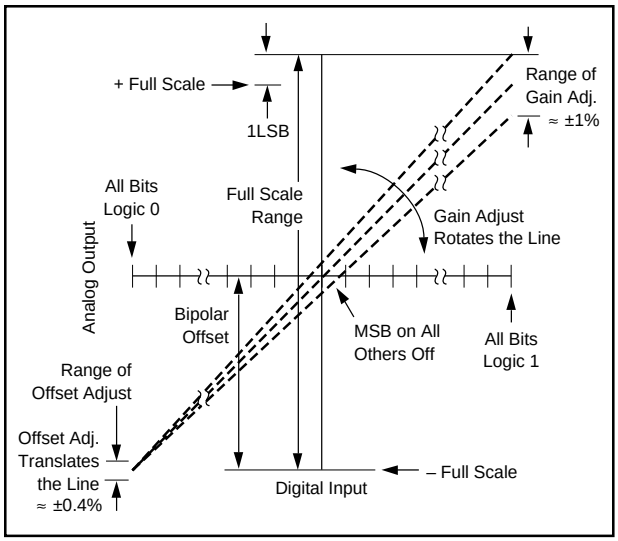


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Gain Adjustment

For either unipolar or bipolar operation, apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for calibration values.

DIGITAL INPUT	ANALOG OUTPUT				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FFF_{HEX}	+4.9987V	+9.9976V	+2.4987V	+4.9976V	+9.9951V
800_{HEX}	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+2.4987V	+4.9976V	–0.0013V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	0.0000V	–2.5000V	–5.0000V	–10.0000V
1LSB	1.22mV	2.44mV	1.22mV	2.44mV	4.88mV

TABLE II. Calibration Values.

SETTLING TIME PERFORMANCE

The switches, reference and output amplifier of the DAC667 are designed for optimum settling time performance (Figure 4). Figure 4a shows the full scale range step response, V_{OUT} –10V to +10V to –10V, for data input 000_{HEX} to FFF_{HEX} to 000_{HEX}. Figure 4b shows the settling time response at plus full scale (+10V) for an output transition from –10V to +10V. Figure 4c shows the settling time response at minus full scale (–10V) for an output transition from +10V to –10V. Figure 4d shows the major carry glitch response for input code transitions $7FF_{HEX}$ to 800_{HEX} and for 800_{HEX} to $7FF_{HEX}$.

Unlike the Analog Devices AD667, the Burr-Brown DAC667 does not require an external capacitor (C_f = 20pF) across R_{SPAN} to eliminate overshoot. Using the 20pF with the Burr-

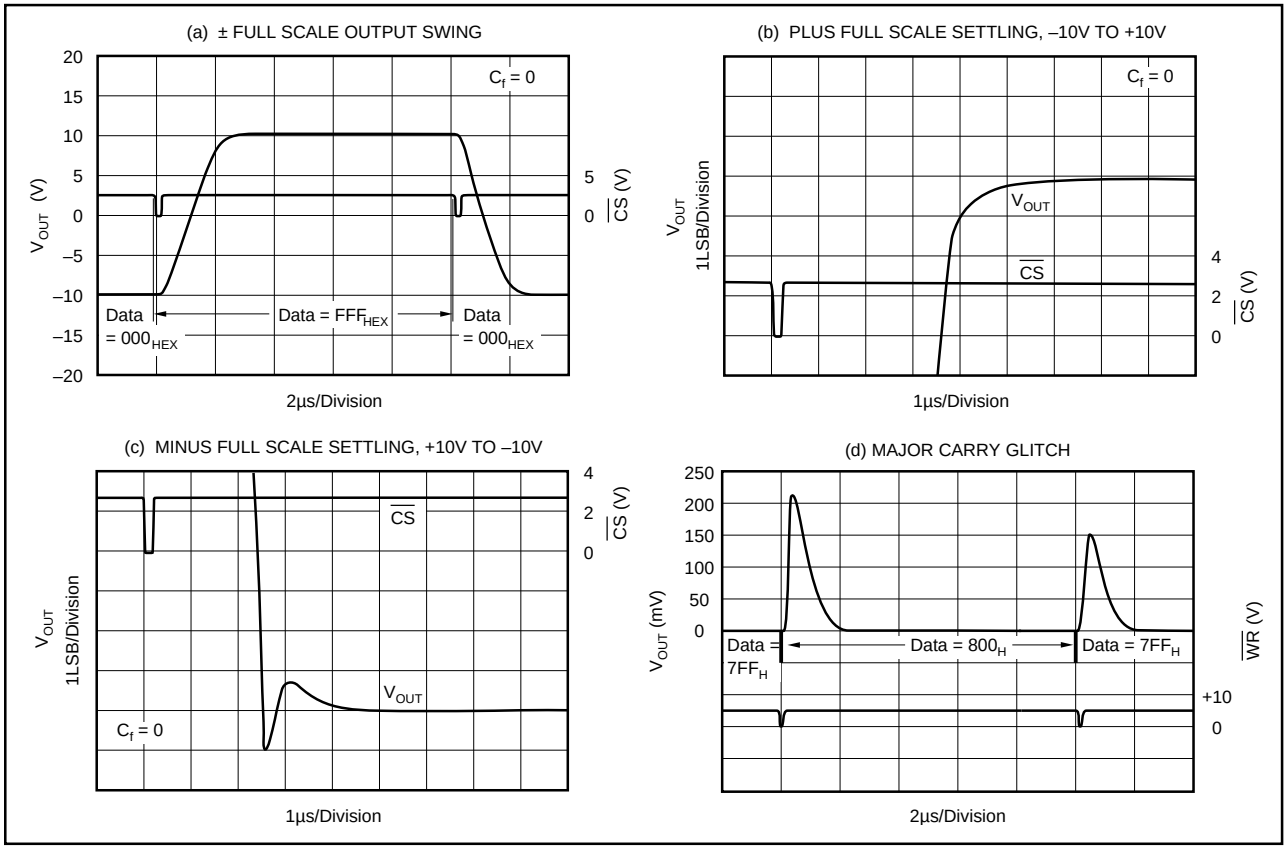


FIGURE 4. Settling Time Performance, Z_{LOAD} = 2kΩ || 500pF.

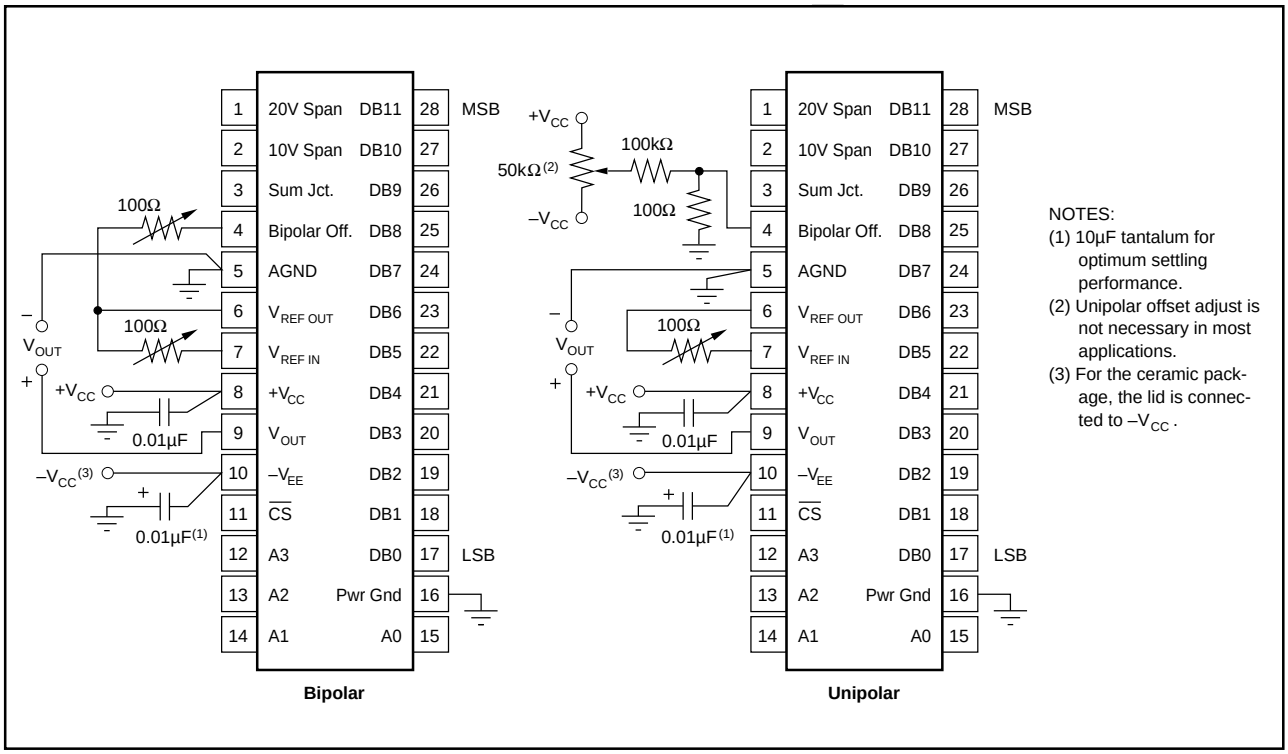


FIGURE 5. Power Supply, Gain and Offset Connections.

Brown DAC667 increases the settling time about one microsecond. The DAC667 settling time is specified at 7µs maximum. The AD667 is specified at 4µs maximum.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the metal lid of the ceramic-packaged DAC667 is connected to $-V_{EE}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Best settling performance occurs using a 1µF to 10µF tantalum capacitor at $-V_{EE}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{EE}$ as well as at $+V_{CC}$. The capacitors should be located close to the DAC667 package.

DAC667 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both power ground (pin 16) and analog ground (AGND, pin 5) be connected directly to a ground plane under the package. If a ground plane is not used, connect the AGND and power ground pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the AGND pin, it is also important to connect the load directly to the AGND pin.

The change in current in the AGND pin due to an input data word change from 000_{HEX} to FFF_{HEX} is only 1mA.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

The DAC667 output amplifier can provide ±10V output swing while operating on ±11.4V supplies. The Analog Devices AD667 requires a minimum of ±12.5V to achieve an output swing of ±10V.

Internal scaling resistors provided in the DAC667 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. Refer to Figures 6, 7 and 8. Connections for various output ranges are shown in Table III.

The internal feedback resistors (5kΩ) and the bipolar offset resistor (9.95kΩ) are trimmed to an absolute tolerance of about ±10%.

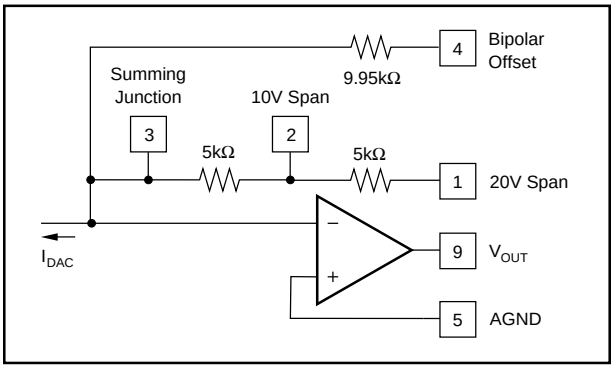


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 9 TO	CONNECT PIN 1 TO	CONNECT PIN 2 TO	CONNECT PIN 4 TO
±10V	Offset Binary	1	9	NC	6 (Through 50Ω fixed or 100Ω trim resistor.)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (Through 50Ω fixed or 100Ω trim resistor.)
±2.5V	Offset Binary	2	3	9	6 (Through 50Ω fixed or 100Ω trim resistor.)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (Or optional trim. See Figure 7.)
0 to +5V	Straight Binary	2	3	9	5 (Or optional trim. See Figure 7.)

TABLE III. Output Voltage Range Connections.

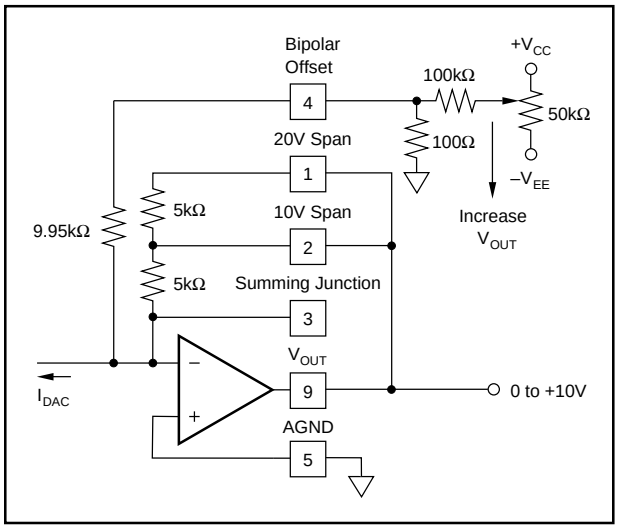


FIGURE 7. 0 to +10V Unipolar Voltage Output.

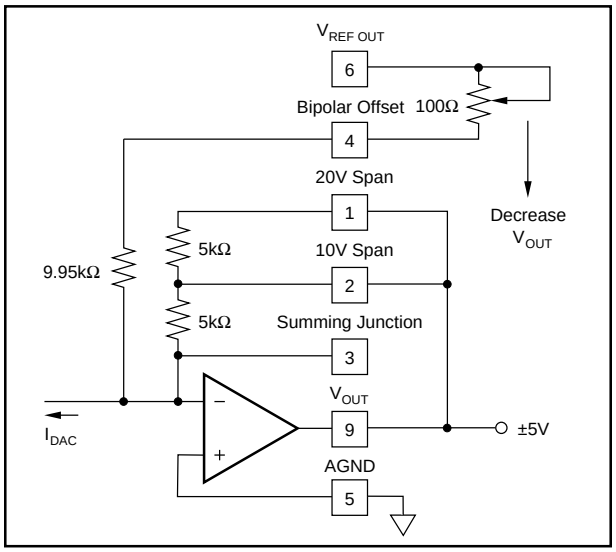


FIGURE 8. ±5V Bipolar Voltage Output.

MICROCOMPUTER BUS INTERFACING

8-BIT BUS INTERFACE

The DAC667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats. Data formats for 8-bit buses are illustrated in Figure 9.

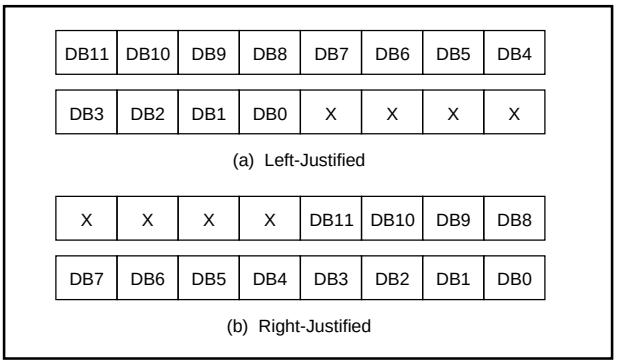


FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

Whenever a 12-bit D/A is loaded from an 8-bit bus, two bytes are required. If the software program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

Figure 10 shows an addressing scheme for use with a DAC-667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the DAC667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

Right-justified data can also be accommodated as shown in Figure 11. The DAC667 still occupies two adjacent locations in the processor's memory map. Location X01 loads the eight LSBs and location X10 loads the four MSBs and updates the output.

12- AND 16-BIT BUS INTERFACES

For operation with 12- and 16-bit buses, all four address lines (A0 through A3) are connected to logic 0, and the latch is enabled by $\overline{CS}$ asserted low. The DAC667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the DAC667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering. See Figure 12.

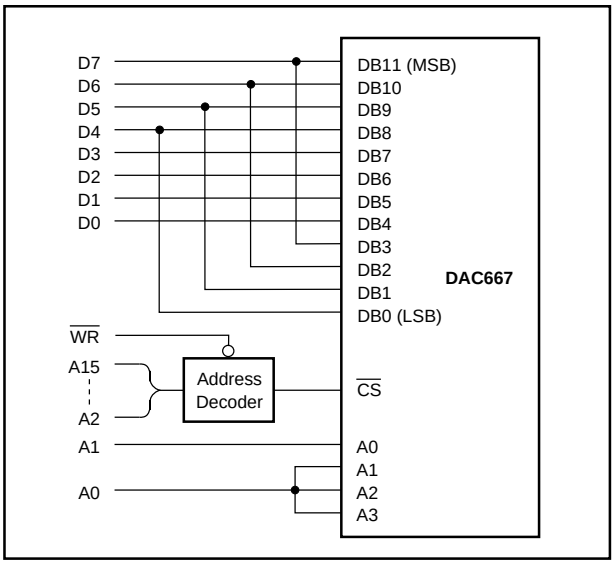


FIGURE 10. Left-Justified 8-Bit Bus Interface.

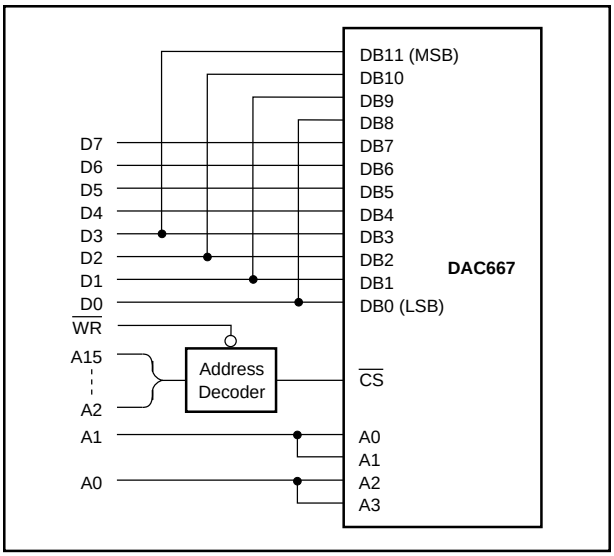


FIGURE 11. Right-Justified 8-Bit Bus Interface.

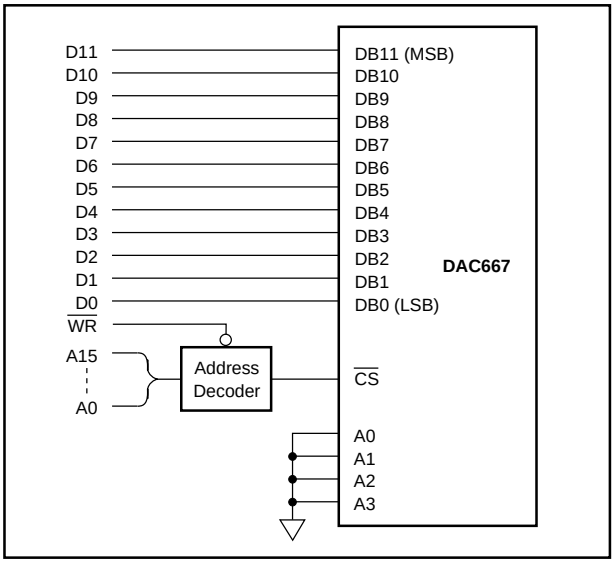
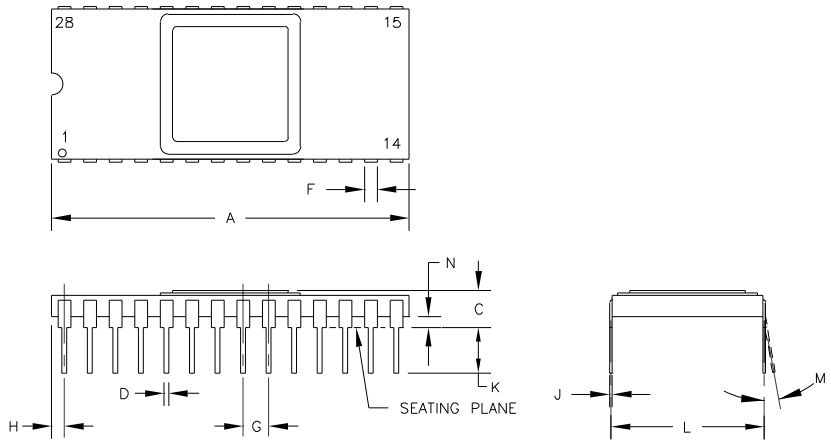


FIGURE 12. Connections for 12- and 16-Bit Bus Interface.

PACKAGE DRAWINGS

Package Number 149 - 28-Pin Hermetic Ceramic DIP

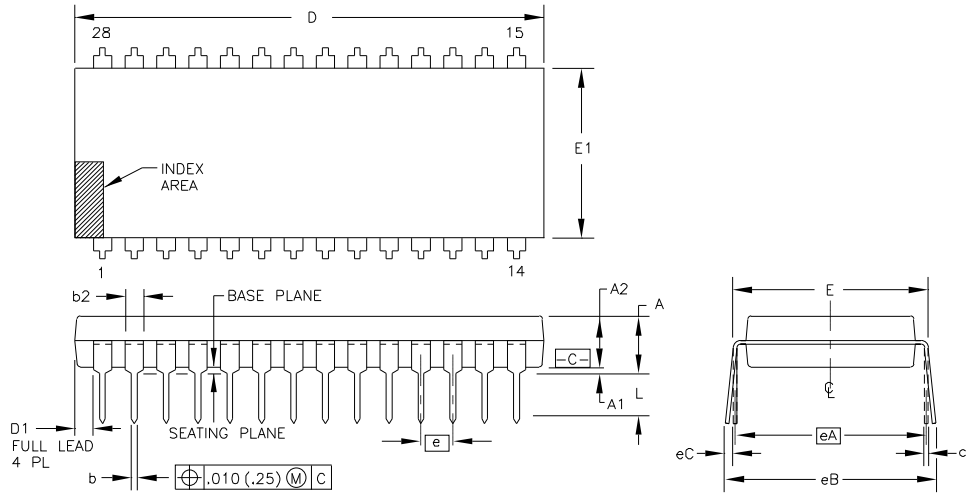


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	1.386	1.414	35.20	35.92	
C	.115	.175	2.92	4.45	
D	.015	.021	0.38	0.53	
F	.035	.060	0.89	1.52	
G	.100	BASIC	2.54	BASIC	
H	.036	.064	0.91	1.63	
J	.008	.012	0.20	0.30	
K	.120	.240	3.05	6.10	
L	.600	BASIC	15.24	BASIC	
M	--	10°	--	10°	
N	.025	.060	0.64	1.52	

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ149 | REV.: B
JEDEC NUMBER: MO-038 WITH EXCEPTIONS

Package Number 215 - 28-Pin Plastic, Double-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.250	--	6.35	3
A1	.015	--	0.38	--	3
A2	.125	.195	3.18	4.95	
b	.014	.022	0.36	0.56	
b2	.030	.070	0.76	1.78	9
c	.008	.015	0.20	0.38	
D	1.380	1.565	35.05	39.75	4
D1	.005	--	0.13	--	4
E	.600	.625	15.24	15.88	5
E1	.485	.580	12.32	14.73	4
e	.100	BASIC	2.54	BASIC	
eA	.600	BASIC	15.26	BASIC	5
eB	--	.700	--	17.78	6
eC	.000	.060	0.00	1.52	6
L	.115	.200	2.92	5.08	3
N	28		28		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ215 | REV.: J
JEDEC NUMBER: MS-011-AB