

DAC4815

Quad 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY: $\pm 1/2$ LSB max
- BIPOLAR OUTPUT
- CLEAR/RESET TO BIPOLAR ZERO

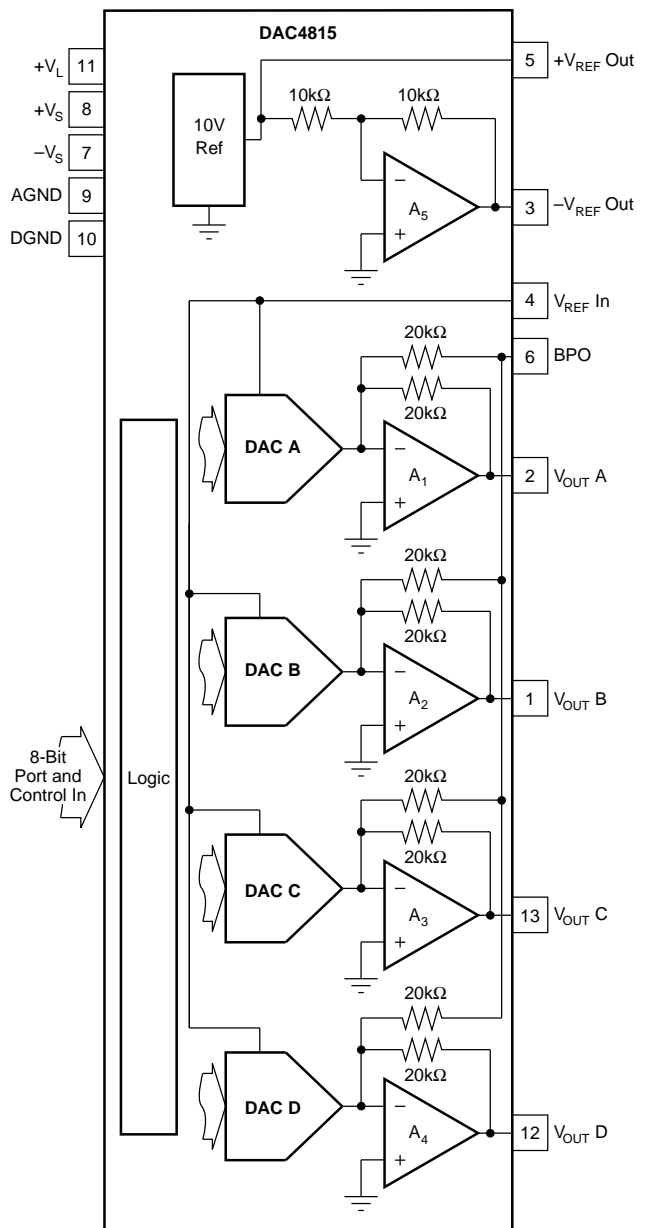
DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar $\pm 10V$ output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the $-40^{\circ}C$ to $+85^{\circ}C$ extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



SPECIFICATIONS, Guaranteed over $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise specified.

ELECTRICAL

Specifications as shown for $V_S = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_L = +5\text{V}$, and $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS Resolution V_{IH} (Input High Voltage) V_{IL} (Input Low Voltage) I_{IN} (Input Current) C_{IN} (Input Capacitance)	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	12 2 0		5 0.8 ± 1 ± 10	*		*	Bits V V μA μA pF
ACCURACY Integral, Relative Linearity ⁽¹⁾ Differential Nonlinearity ⁽²⁾ Bipolar Zero Error Gain Error Power Supply Sensitivity ⁽³⁾	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ With Internal or External 10.0V Ref $V_S = \pm 11.4\text{V}$ to $\pm 18\text{V}$ $V_L = +4.5\text{V}$ to $+5.5\text{V}$		$\pm 1.5/-1$ ± 20	± 1 ± 1 ± 0.2 30		± 10	$\pm 1/2$ * ± 1 mV ± 0.15 *	LSB LSB LSB % ppmFSR/V
TEMPERATURE DRIFT Gain Drift Bipolar Zero Drift			± 5 ± 5	± 30 ± 15		*	± 20 ± 8	ppm/ $^{\circ}\text{C}$ ppmFSR/ $^{\circ}\text{C}$
REFERENCE OUTPUT Output Voltage Reference Drift Output Current Max Load Capacitance (For Stability) Short Circuit Current Load Regulation (ΔV_{OUT} vs ΔI_{LOAD}) Supply Regulation (ΔV_{OUT} vs ΔV_S) -REFERENCE OUTPUT, Inverter -10V Reference -10V Reference Drift DC Output Impedance Output Current Max Load Capacitance (For Stability) Short Circuit Current	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	+9.980 +10/-5 +5/-5	+10 ± 2 500 ± 20 40 ± 5	+10.020 ± 30 -9.980 ± 30	+9.985 * *	*	+10.015 ± 20 -9.985 ± 20	V ppm/ $^{\circ}\text{C}$ mA mA pF mA ppm/mA ppm/V V ppm/ $^{\circ}\text{C}$ Ω mA pF mA
REFERENCE INPUT Reference Input Resistance Inverter Input Resistance BPO Input Resistance Reference Input Range		1.75 7 3.5	2.5 10 5	± 10	*	*	*	k Ω k Ω k Ω V
ANALOG SIGNAL OUTPUTS Voltage Range DC Output Impedance Output Current Max Load Capacitance (For Stability) Short Circuit Current	V_{OUT}	$-V_S + 1.4$ ± 5	 0.1 500 ± 30	$+V_S - 1.4$	*	*	*	V Ω mA pF mA
DYNAMIC PERFORMANCE ⁽⁴⁾ Settling Time Slew Rate Small-Signal Bandwidth	$C_L = 100\text{pF}$ To 1/2 LSB of Full Scale		3.5 10 3	10		*	*	μs V/ μs MHz
ANALOG GROUND CURRENT (Code Dependent)			± 4			*		mA
DIGITAL CROSSTALK	Full Scale Transition $C_L = 100\text{pF}$		3			*		nV-s
DIGITAL-TO-ANALOG GLITCH IMPULSE			30			*		nV-s
POWER SUPPLY $+V_S$ and $-V_S$ $+V_L$ $+I_S$ $-I_S$ $+I_L$ $+L$ Total Power, All DACs	Digital Inputs = 0V or $+V_L$ Digital Inputs = V_{IL} or V_{IH}	± 11.4 4.5	± 15 5 +20 -20 0.4	± 18 5.5 +24 -25.5 2 10 753	*	*	*	V V mA mA mA mA mA mW

SPECIFICATIONS (CONT), Guaranteed over $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise specified.

ELECTRICAL

Specifications as shown for $V_S = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_L = +5\text{V}$, and $R_L = 2\text{k}\Omega$ unless otherwise noted.

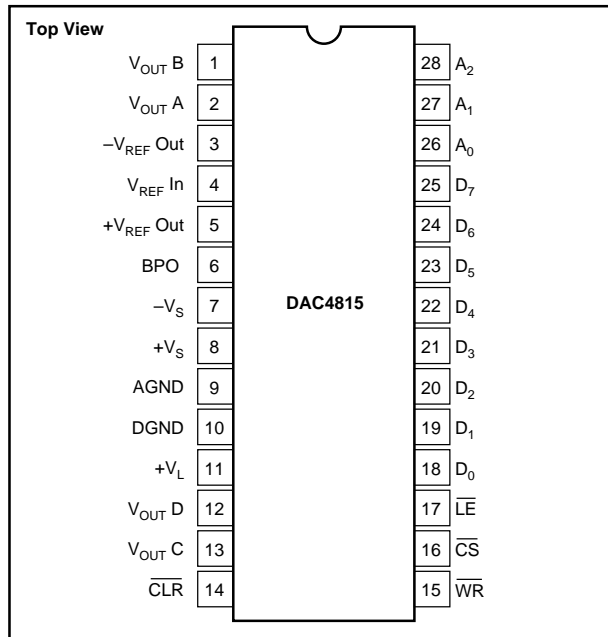
PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specified Operating Thermal Resistance, θ_{JA}		-40		+85	*		*	$^{\circ}\text{C}$
		-40		+85	*		*	$^{\circ}\text{C}$
			75			*		$^{\circ}\text{C}/\text{W}$

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	$V_{OUT\ B}$	Analog output voltage, DAC B	28	A_2	Address line 2 input
2	$V_{OUT\ A}$	Analog output voltage, DAC A	27	A_1	Address line 1 input
3	$-V_{REF\ Out}$	Negative reference voltage output (-10V output)	26	A_0	Address line 0 input
4	$V_{REF\ In}$	\pm Reference voltage input	25	D_7	Data bit 7 input
5	$+V_{REF\ Out}$	Positive reference voltage output (+10V output)	24	D_6	Data bit 6 input
6	BPO	Bipolar offset input, DAC A, B, C, and D	23	D_5	Data bit 5 input
7	$-V_S$	Negative analog power supply, -15V input	22	D_4	Data bit 4 input
8	$+V_S$	Positive analog power supply, +15V input	21	D_3	Data bit 3 input
9	AGND	Analog common	20	D_2	Data bit 2 input
10	DGND	Digital common	19	D_1	Data bit 1 input
11	$+V_L$	Positive logic power supply, +5V input	18	D_0	Data bit 0 input
12	$V_{OUT\ D}$	Analog output voltage, DAC D	17	\overline{LE}	Latch data enable, DAC A, B, C, and D
13	$V_{OUT\ C}$	Analog output voltage, DAC C	16	\overline{CS}	Chip select enable, DAC A, B, C, and D
14	\overline{CLR}	Asynchronous input reset to zero	15	WR	Write input, DAC A, B, C, and D

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, -18V
AGND to DGND	$\pm 0.3\text{V}$
Any digital input to GND	-0.3V, $+V_L$ +0.3V
Ref In to AGND	$\pm 25\text{V}$
Ref In to DGND	$\pm 25\text{V}$
Storage Temperature Range	-55°C to $+125^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
Junction Temperature	$+155^{\circ}\text{C}$
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC4815AP	± 1
DAC4815BP	$\pm 1/2$

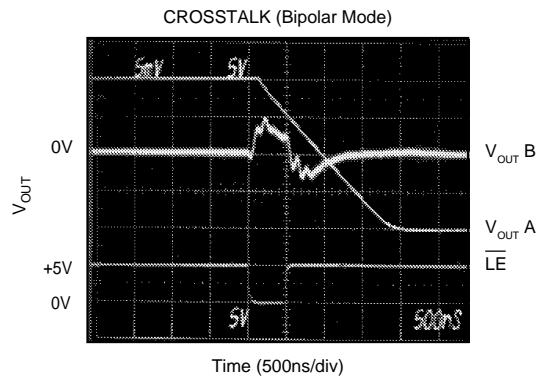
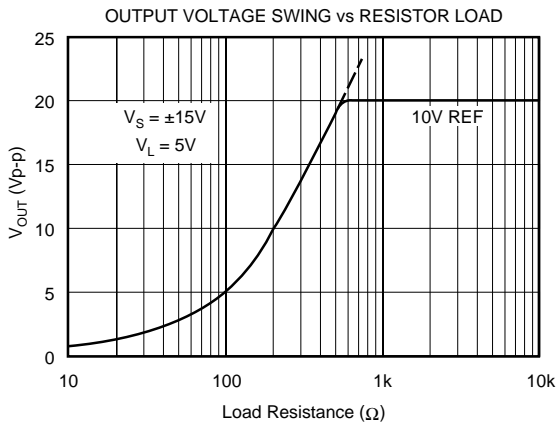
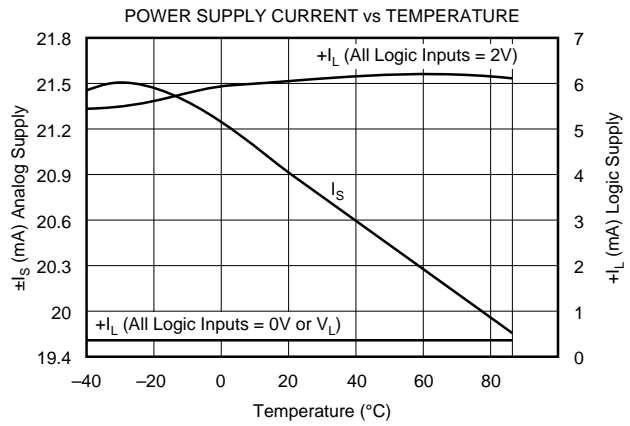
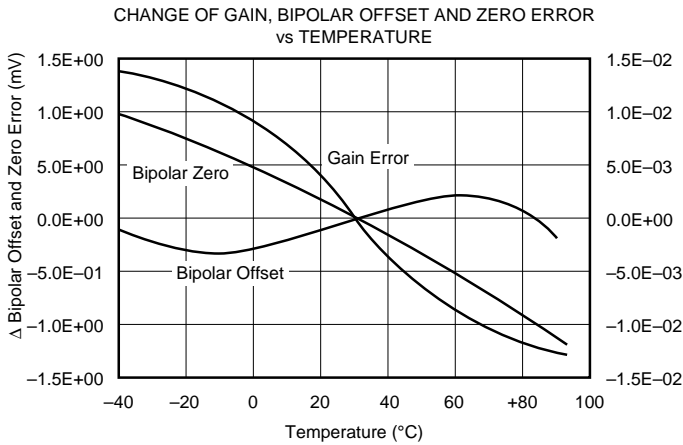
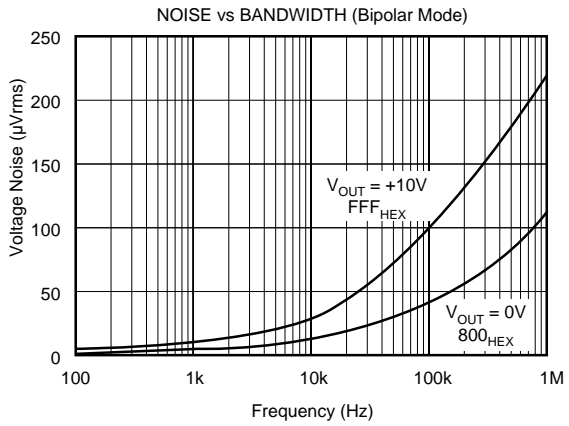
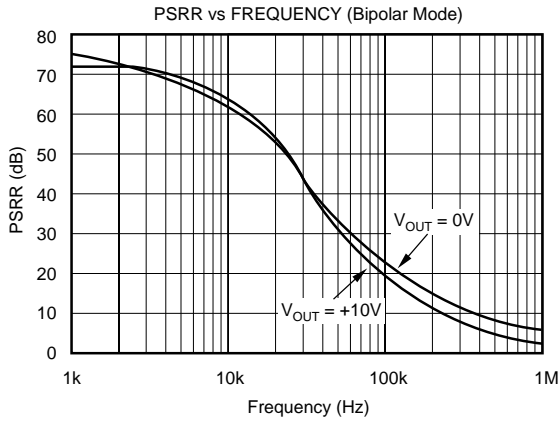
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
DAC4815AP	28-Pin Plastic DIP	215
DAC4815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_L = +5\text{V}$ unless otherwise noted.

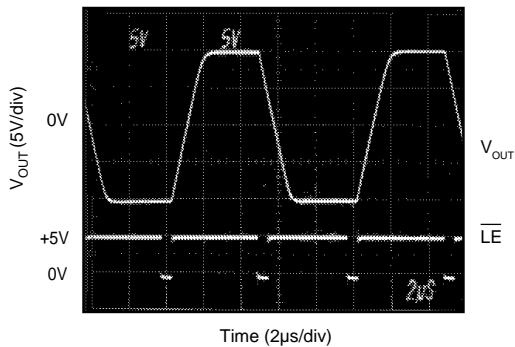


NOTE: Crosstalk is dominated by digital crosstalk/feedthrough of \overline{LE} signal.

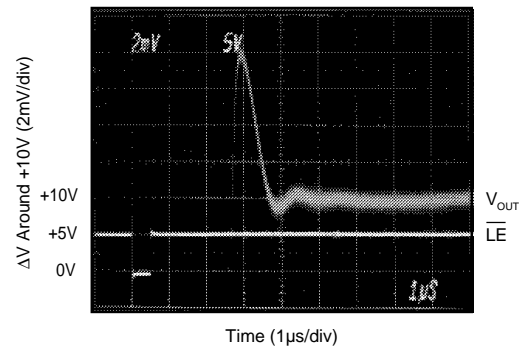
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 12\text{V}$ or $\pm 15\text{V}$, $V_L = +5\text{V}$ unless otherwise noted.

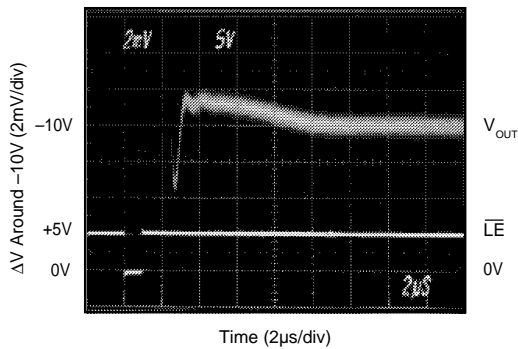
FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)



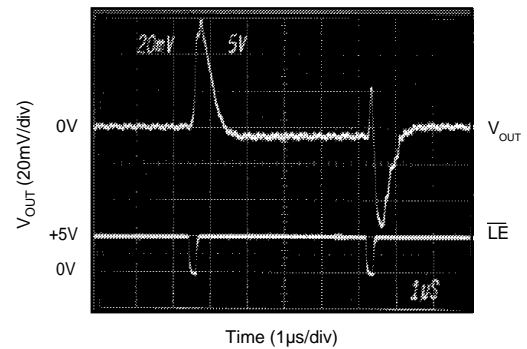
SETTLING TIME
BIPOLAR (-10V to +10V)



SETTLING TIME
BIPOLAR (+10V to -10V Step)

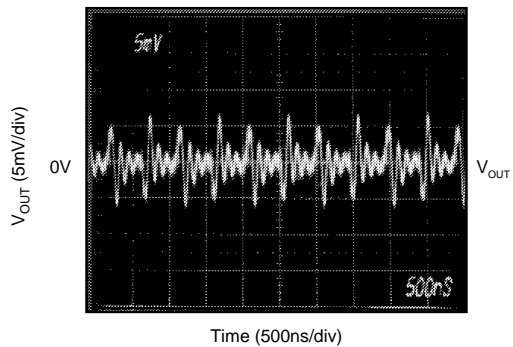


MAJOR CARRY GLITCH



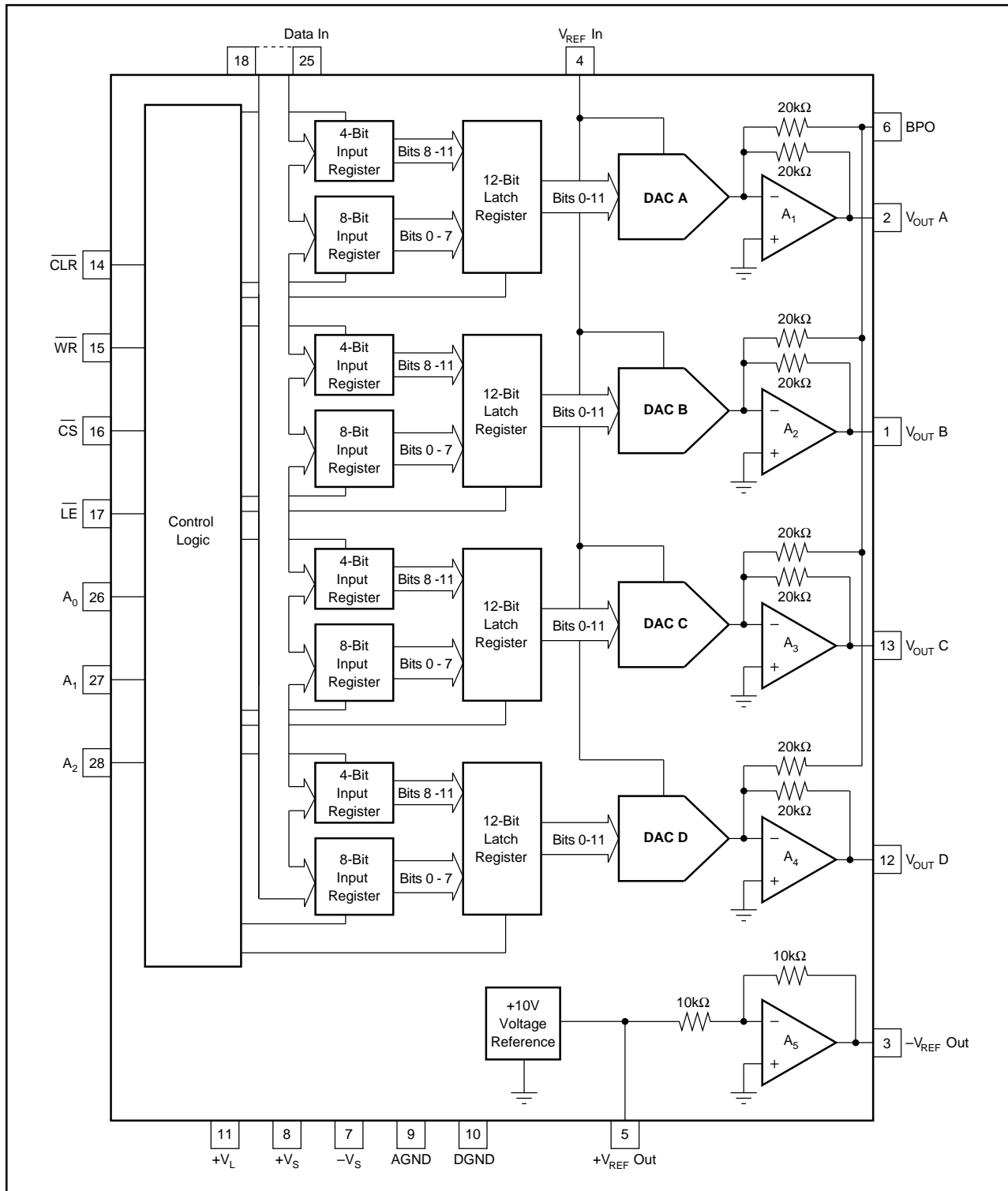
NOTE: Data transition 800_{HEX} to 7FF_{HEX}.

DIGITAL FEEDTHROUGH



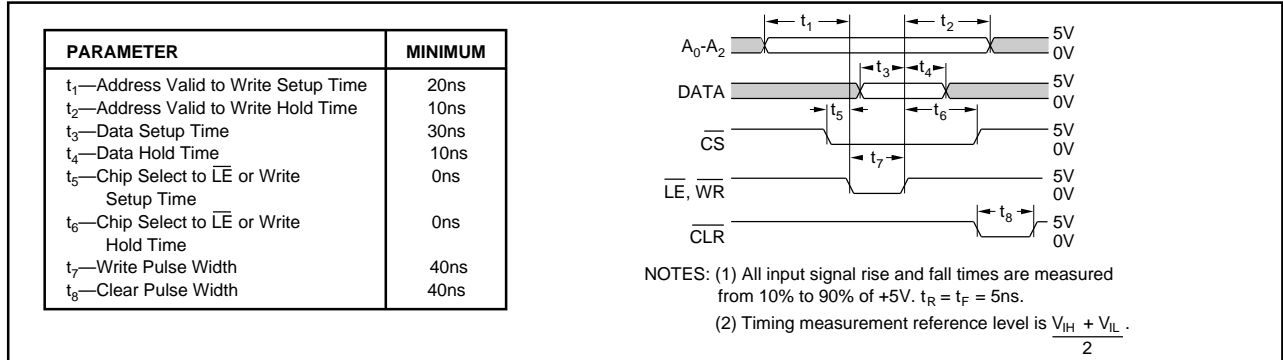
DAC output noise due to activity on digital inputs with latch disabled.

FUNCTIONAL BLOCK DIAGRAM, DAC4815 — Quad 12-bit DAC, 8-bit Port



TIMING CHARACTERISTICS

+V_L = +5V, T_A = -40°C to +85°C.



INTERFACE LOGIC TRUTH TABLE

CLR	$\overline{\text{LE}}$	$\overline{\text{CS}}$	WR	A ₂	A ₁	A ₀	FUNCTION
1	1	0	0	0	0	0	DAC A LS input register loaded with D7-D0(LSB)
1	1	0	0	0	0	1	DAC A MS input register loaded with D3(MSB)-D0
1	1	0	0	0	1	0	DAC B LS input register loaded with D7-D0(LSB)
1	1	0	0	0	1	1	DAC B MS input register loaded with D3(MSB)-D0
1	1	0	0	1	0	0	DAC C LS input register loaded with D7-D0(LSB)
1	1	0	0	1	0	1	DAC C MS input register loaded with D3(MSB)-D0
1	1	0	0	1	1	0	DAC D LS input register loaded with D7-D0(LSB)
1	1	0	0	1	1	1	DAC D MS input register loaded with D3(MSB)-D0
1	0	0	1	X	X	X	All DAC registers updated simultaneously from input registers
1	0	0	0	X	X	X	All DAC registers are transparent
1	X	1	X	X	X	X	No data transfer
1	1	X	1	X	X	X	No data transfer
0	X	X	X	X	X	X	Input registers cleared = 000 _{HEX} , DAC registers = 800 _{HEX}

NOTE: X = Don't care.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4815 are TTL and 5V CMOS compatible. Input codes for the DAC4815 are BOB (Bipolar Offset Binary). See Figure 3 for ±10V bipolar connection.

BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	BIPOLAR (BOB)
FFF _{HEX}	+Full Scale
800 _{HEX}	Zero
7FF _{HEX}	Zero - 1 LSB
000 _{HEX}	-Full Scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX}.

GAIN ERROR

The deviation of the output voltage span (V_{MAX} - V_{MIN}) from the ideal span of 20V - 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV-s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the \overline{WR} signal is brought low. The data are latched in the input register when the \overline{WR} goes high. Data are then transferred from the input registers to the DAC latch registers by bringing \overline{LE} low. The data are latched in the DAC latch registers when \overline{LE} goes high. All DACs are updated simultaneously.

When \overline{CLR} is brought low, the input registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX} . If \overline{LE} is brought low after \overline{CLR} the DACs are updated with 000_{HEX} resulting in -10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener $+10.0\text{V}$ reference and a -10V reference are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R , $2R$ ladder network is driven by a voltage reference at V_{REF} . Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to $\pm 10\text{V}$.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB} , compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

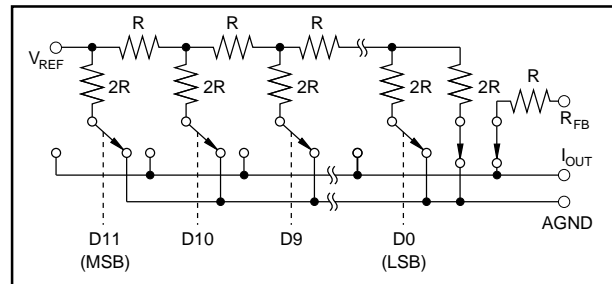


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

POWER SUPPLY CONNECTIONS

The DAC4815 is specified for operation with power supplies of $V_L = +5\text{V}$ and $V_S = \text{either } \pm 12\text{V} \text{ or } \pm 15\text{V}$. Even with the V_S supplies at $\pm 11.4\text{V}$ the DACs can swing a full $\pm 10\text{V}$. Power supply decoupling capacitors ($1\mu\text{F}$ tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

$\pm 10\text{V}$ OUTPUT RANGE CONNECTION

For a $\pm 10\text{V}$ bipolar output connect the DAC4815 as shown in Figure 3.

CONNECTION TO DIGITAL BUS

DAC4815s can easily be connected to a μ processor bus. Decode your address lines to derive the control signals shown in Figure 4. Only one $\overline{\text{LATCH}}$ signal is required for a system where all DAC4815s are updated simultaneously. If you want to update DAC4815s independently, use separate $\overline{\text{LATCH}}$ signals. The $\overline{\text{LATCH}}$ and $\overline{\text{WRITE}}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

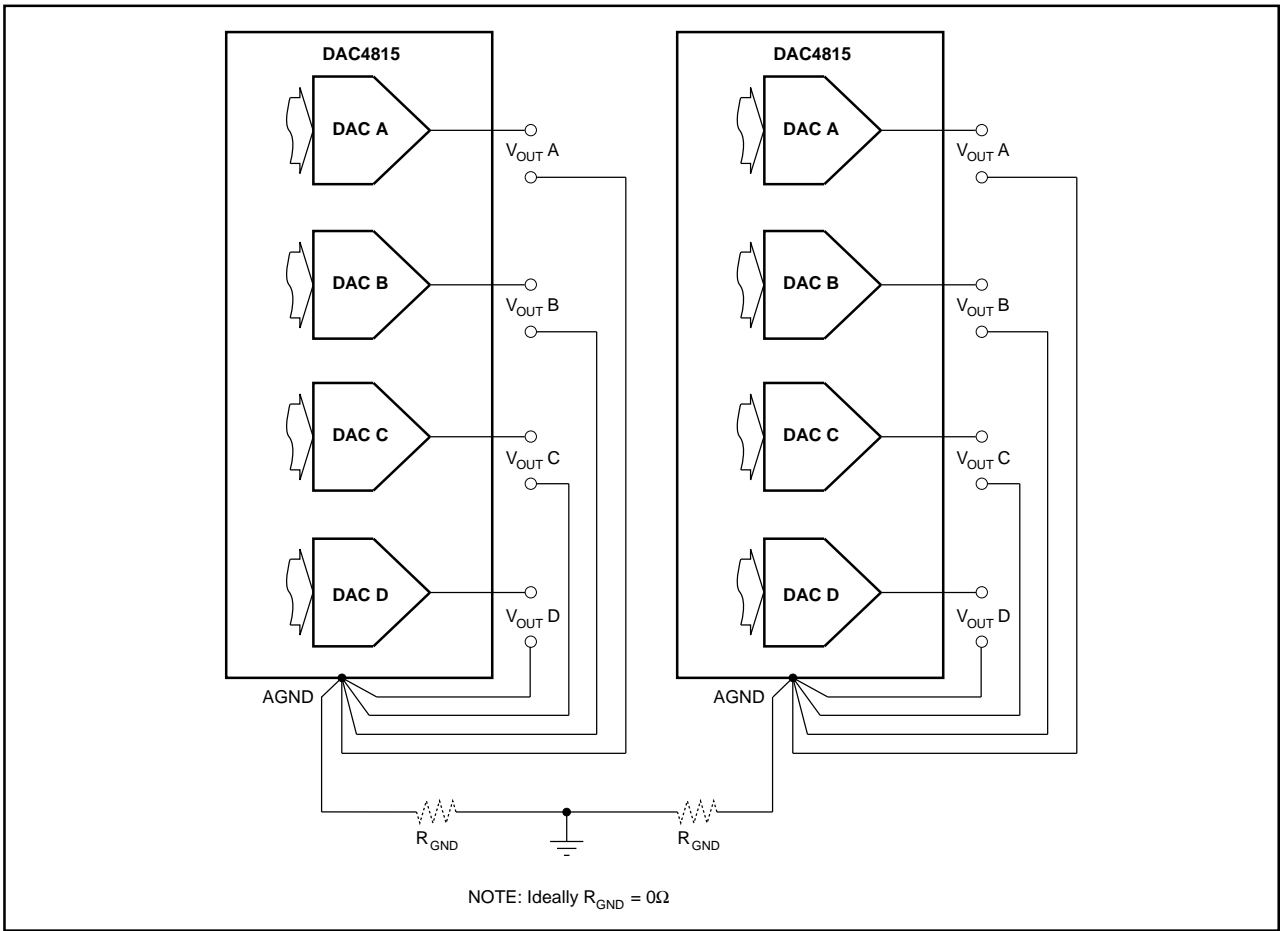


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

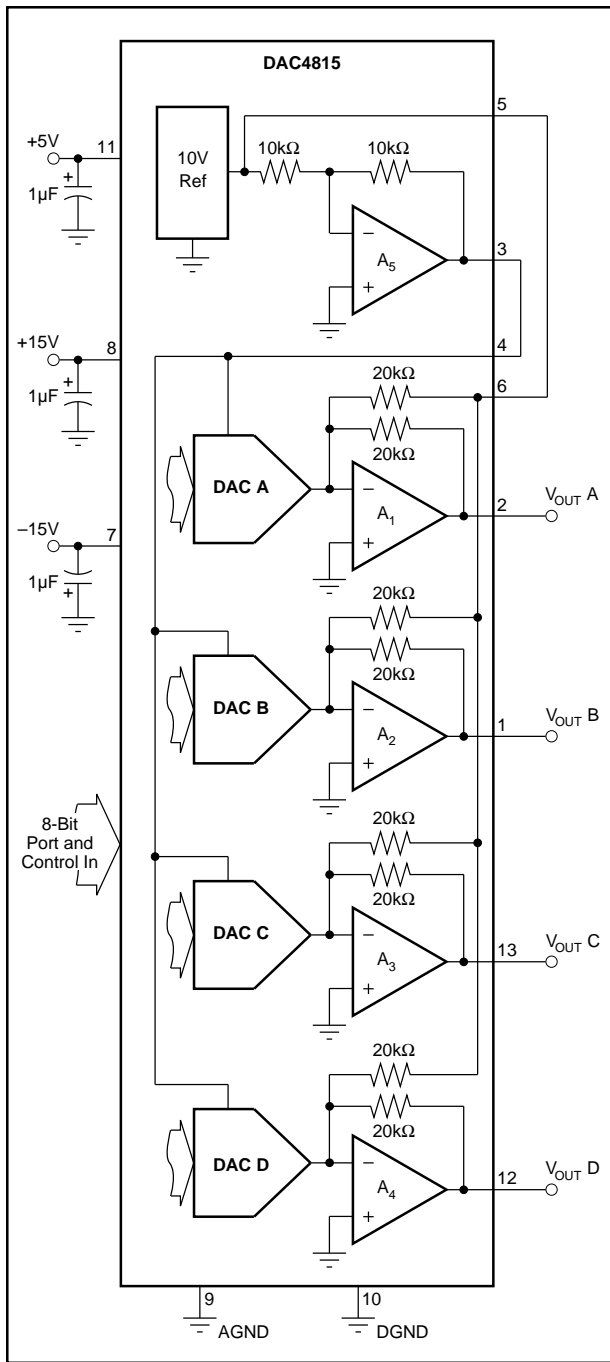


FIGURE 3. Analog Connections for ±10V DAC Output.

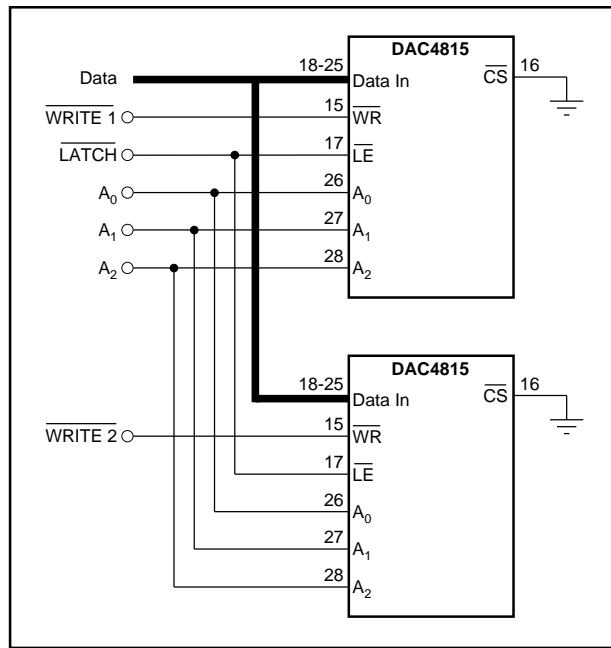
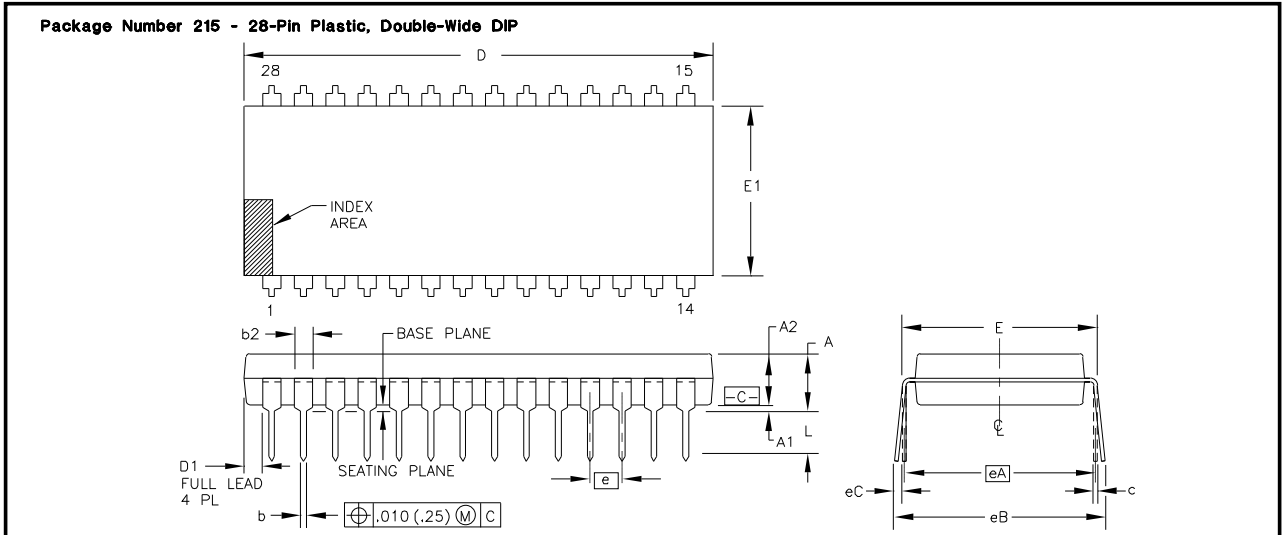


FIGURE 4. Logic Connections for Multiple DAC4815 Packages.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PACKAGE DRAWING



DIM	INCHES		MILLIMETERS		NOTE	DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	--	.250	--	6.35	3	L	.115	.200	2.92	5.08	3
A1	.015	--	0.38	--	3	N	28	28			7
A2	.125	.195	3.18	4.95							
b	.014	.022	0.36	0.56							
b2	.030	.070	0.76	1.78	9						
c	.008	.015	0.20	0.38							
D	1.380	1.565	35.05	39.75	4						
D1	.005	--	0.13	--	4						
E	.600	.625	15.24	15.88	5						
E1	.485	.580	12.32	14.73	4						
e	.100	BASIC	2.54	BASIC							
eA	.600	BASIC	15.26	BASIC	5						
eB	--	.700	--	17.78	6						
eC	.000	.060	0.00	1.52	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM $\overline{C-C}$.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.

8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: Z2215 REV.: J
 JEDEC NUMBER: MS-011-AB