

# AN7348K

## Dual Record/Playback Pre-Amplifier IC for Double Cassette

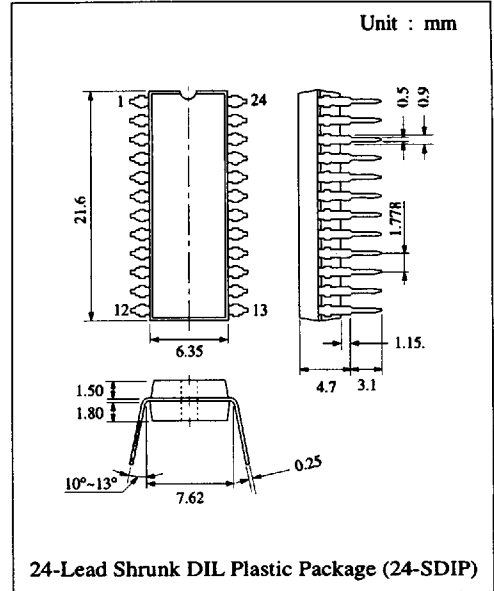
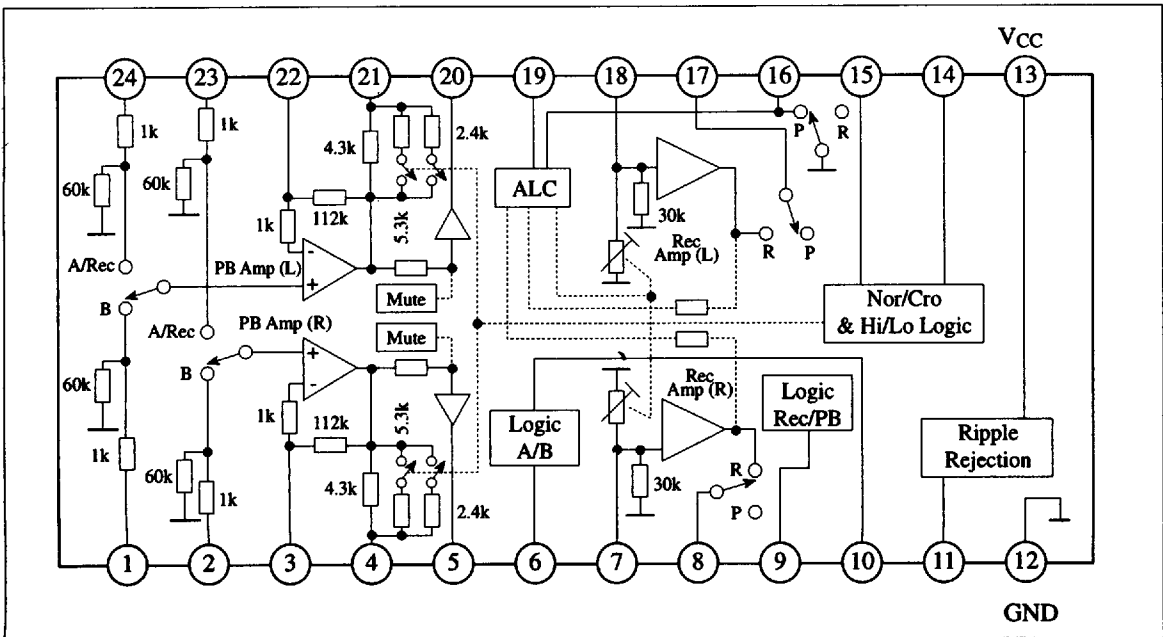
### ■ Description

The AN7348K is a monolithic integrated circuit designed for double cassette recorder. It has dual channel PB / Rec amplifier with ALC function. Tape A ( PB only ) and Tape B ( PB / Rec ) select, Normal / Chrome select, Normal / High speed dubbing select and Rec / PB selection are easily controlled by 4 pins. It requires no external FET switches at PB amp. input and Rec amp. output. External components are also minimized. In addition, this IC has low susceptibility to EMC.

### ■ Features

- Built-in Normal / Chrome equalizer for PB amplifier
- Built-in Normal / High speed equalization for PB amplifier
- Built-in Tape A/B switching
- Built-in Rec / PB select
- ALC function for recording
- Wide operating supply voltage range :  
Vcc = 3.6V ~ 12V
- Can connect IC directly to tape head. No external FET switches is required
- Minimum switching noise.

### ■ Block Diagram



### ■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V <sub>CC</sub>	12.4	V
Supply Current	I <sub>CC</sub>	40	mA
Power Dissipation	P <sub>D</sub>	500	mW
Operating Ambient Temperature	T <sub>opr</sub>	-20 ~ +75	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +150	°C

Operating Supply Voltage Range: V<sub>CC</sub> = 3.6V ~ 12.0V

### ■ Electrical Characteristics (V<sub>CC</sub>=5V, Ta=25°C)

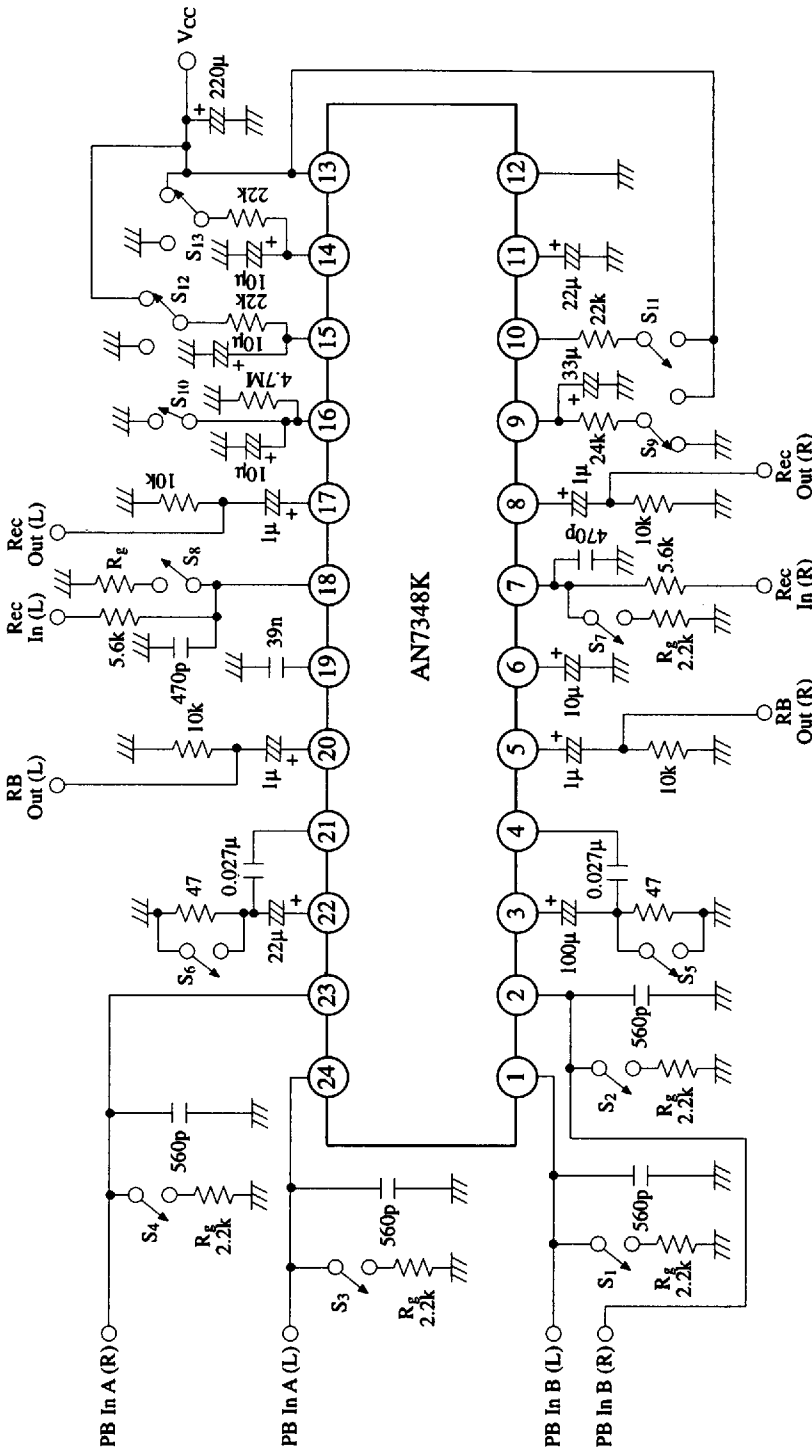
Item	Symbol	Condition	min.	typ.	max.	Unit
Quiescent Circuit Current (REC)	I <sub>CQrec</sub>	V <sub>in</sub> = 0V	12.0	18	24	mA
<b>Playback Amplifier</b>						
Close Loop Gain	G <sub>VC(P)</sub>	V <sub>in</sub> = 5.6mVrms	40	42.5	45	dB
Open-Loop Gain	G <sub>VO(P)</sub>	V <sub>in</sub> = 89μVrms	75	81		dB
Input Noise	V <sub>ni(P)</sub>	R <sub>g</sub> = 2.2kΩ, DIN/AUDIO, V <sub>in</sub> = V <sub>no</sub> / G <sub>VC</sub>		1.8	2.5	μV
Total Harmonic Distortion	THD <sub>(P)</sub>	V <sub>O</sub> = 1Vrms, BPF		0.05	0.1	%
Max. Output Voltage	V <sub>O(P)</sub>	THD = 3%, BPF	1.4	1.7		Vrms
Channel Balance	CB <sub>(P)</sub>	V <sub>in</sub> = 5.6mVrms	-1.5	0	1.5	dB
Channel Crosstalk	CT <sub>C(P)</sub>	V <sub>in</sub> = 5.6mVrms, R <sub>g</sub> = 2.2kΩ, DIN/AUDIO	55	65		dB
Source Crosstalk	CT <sub>S(P)</sub>	V <sub>in</sub> = 5.6mVrms, R <sub>g</sub> = 2.2kΩ, DIN/AUDIO	55	65		dB
<b>Playback EQ</b>						
120μs / 70μs ΔGain*1	ΔG <sub>vc1</sub>	V <sub>in</sub> =10mVrms, f=10kHz	4	4.6	5.2	dB
1x / 2x Dubbing ΔGain*2	ΔG <sub>vc2</sub>	V <sub>in</sub> =22mVrms, f=10kHz	4	4.6	5.2	dB
<b>Record Amplifier ALC OFF</b>						
Output Noise Voltage	V <sub>no(R)</sub>	R <sub>g</sub> =1.0kΩ, DIN Audio		220	550	μV
Closed-Loop Gain	G <sub>VC(R)</sub>	V <sub>in</sub> =12mVrms	35.5	38.5	42	dB
Total Harmonic Distortion	THD <sub>(R)</sub>	V <sub>O</sub> =1.0Vrms, BPF		0.05	0.17	%
Max. Output Voltage	V <sub>O(R)</sub>	THD=3%, BPF	1.4	1.8		V
Channel Crosstalk	CT <sub>C(R)</sub>	V <sub>in</sub> =8mVrms, R <sub>g</sub> =1.0kΩ, Din Audio	55	66		dB
<b>ALC (2 Channel Input) ALC ON</b>						
ALC Voltage	V <sub>ALC</sub>	R <sub>ext</sub> =5.6kΩ, Dual i/p, V <sub>in</sub> =12mVrms	0.75	1.0	1.37	Vrms
ALC Range	W <sub>ALC</sub>	R <sub>ext</sub> =5.6kΩ, from V <sub>in</sub> =10mV to V <sub>O</sub> =+3dB	35	51		dB
ALC Channel Balance	CB <sub>(ALC)</sub>	R <sub>ext</sub> =5.6kΩ, V <sub>in</sub> =12mVrms	-2	0	2	dB
<b>Playback Mode</b>						
PB to Rec Crosstalk*3	CT <sub>R/P</sub>	V <sub>in</sub> =12mVrms at Rec i/p, measure at Rec o/p	70	88		dB

Note : \*1 ΔG<sub>vc1</sub> = (G<sub>vc</sub> at 120μs) - (G<sub>vc</sub> at 70μs)

\*2 ΔG<sub>vc2</sub> = (G<sub>vc</sub> at 1x) - (G<sub>vc</sub> at 2x)

\*3 CT<sub>R/P</sub> = 20log(V<sub>b</sub> (PB mode) + V<sub>b</sub> (REC mode))

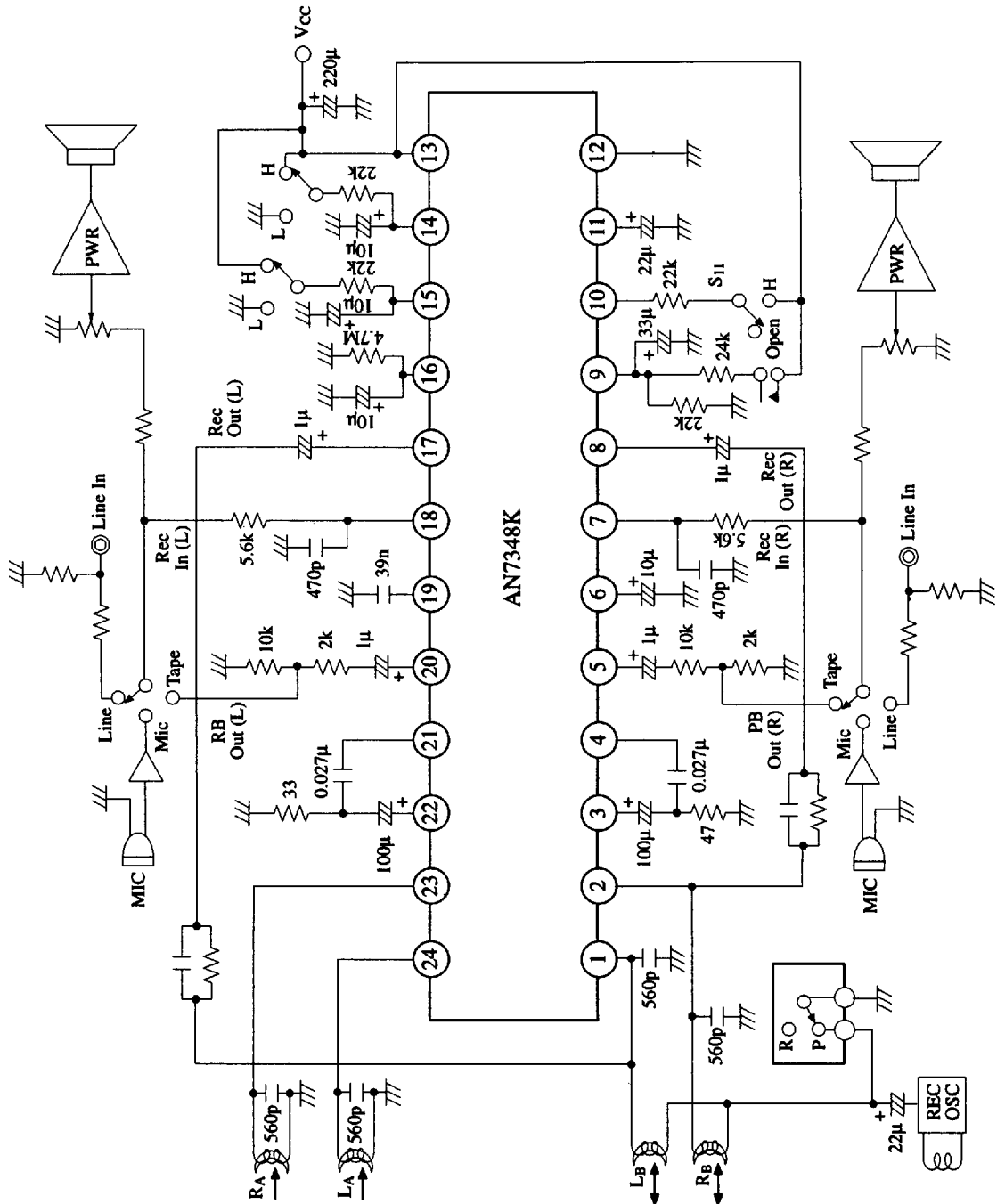
■ Test Circuit



AN7348K

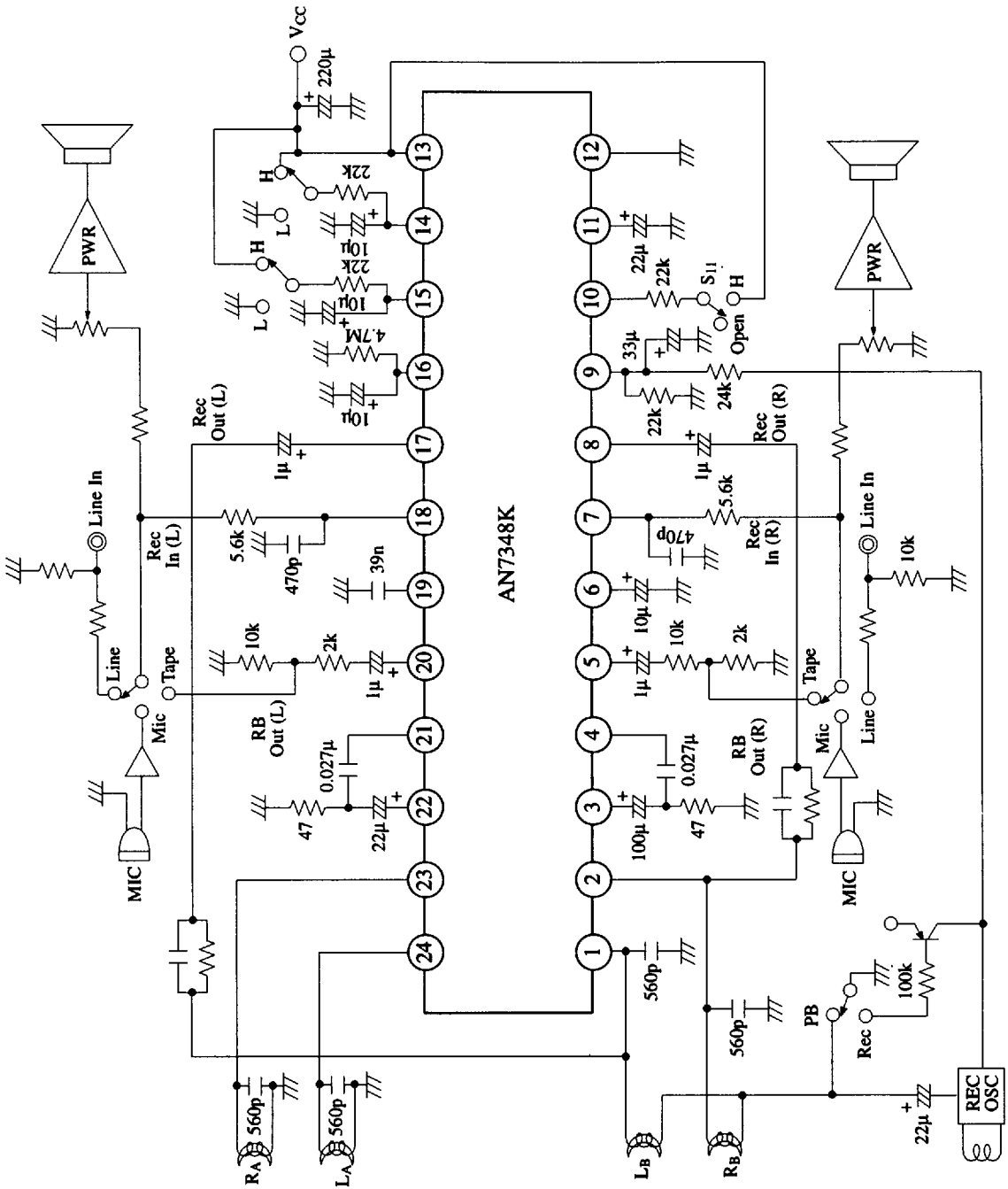
Switch Logic	A/B (S <sub>11</sub> )	Rec / PB (S <sub>9</sub> )	Nor / Cro (S <sub>13</sub> )	Hi / Lo (S <sub>12</sub> )
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Application Circuit - Logic Deck



Logic / Pin	A/B (P10)	Rec / PB (P9)	Nor / Cro (P14)	Hi / Lo (P15)
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Application Circuit 2



Pin / Logic	A/B (P10)	Rec / PB (P9)	Nor / Cro (P14)	Hi / Lo (P15)
High	Tape A	Rec	Chrome	2 x speed
Open	Tape B	PB	Normal	1 x speed
Low	Tape B	PB	Normal	1 x speed

■ Pin Descriptions

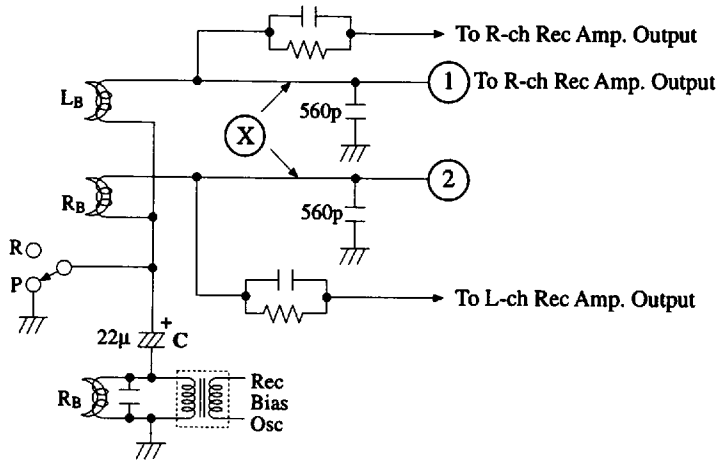
Pin No.	Pin Name	Equivalent Circuit	Description
1	L-ch Playback Amp. Input (B)		<p>Playback amp. input                      Input impedance = 61kΩ                      Pin 1, 2, 23 &amp; 24 = 0V (PB mode)                      *Pin 1, 2 = 2.1V (Rec mode)                      *Pin 23, 24 = 0V (Rec mode)</p>
2	R-ch Playback Amp. Input (B)		
23	R-ch Playback Amp. Input (A)		
24	L-ch Playback Amp. Input (A)		
3	R-ch Playback Negative Feedback		<p>Playback amp. feedback loop                      DC = 0.7V.</p>
22	L-ch Playback Negative Feedback		
4	R-ch Playback Equalization		
21	L-ch Playback Equalization		<p>Low output impedance</p>
5	R-ch Playback Amp Output		
20	L-ch Playback Amp Output		<p>Determines the tape A/B switching time constant with an external capacitor                      DC : 2.8V (pin 10 high)                      DC : 0.0V (pin 10 open)</p>
6	AB Switch τ		
7	R-ch Rec Input		<p>Rec amp input pin                      Input impedance = 30kΩ</p>
18	L-ch Rec Input		
8	R-ch Rec Output		<p>Rec amp output pin                      DC = Vref, Zout = Low (pin 9 High)                      DC = =V, Zout = High (pin 9 Open)</p>
17	L-ch Rec Output		
9	Rec / Playback Switch		<p>Select Rec or playback mode                      0.7V &gt; Threshold &gt; 2.1V</p>

■ Pin Descriptions (Continue)

Pin No.	Pin Name	Equivalent Circuit	Description
10	AB Switch		To select Tape A or Tape B $0.7V > \text{Threshold} > 2.1V$  SW open / 0V 0.7V 1.0V 2.1V Vcc Tape B Tape A PB mute ON
11	Ripple Filter		Connect with a capacitor to minimize ripple from Vcc DC = 4.4V (Vcc = 6V)
12	GND		
13	Vcc		
14	Chrome / Normal		Input to control Playback EQ for Chrome or Normal Tape
15	Hi / Lo		Input to control Playback EQ for High or Low dubbing  Vcc Pin 14 Cro Lo Speed Cro Hi Speed 2.1V Nor Lo Speed Nor Hi Speed 2.1V Pin 15 Vcc
16	ALC $\tau$		Controls the attack and release time of ALC DC = 1.4V → Rec mode DC = 0V → Playback mode
19	ALC Low Cut		ALC comparator circuit reference voltage

■ Supplementary Explanation

1) Recording mode

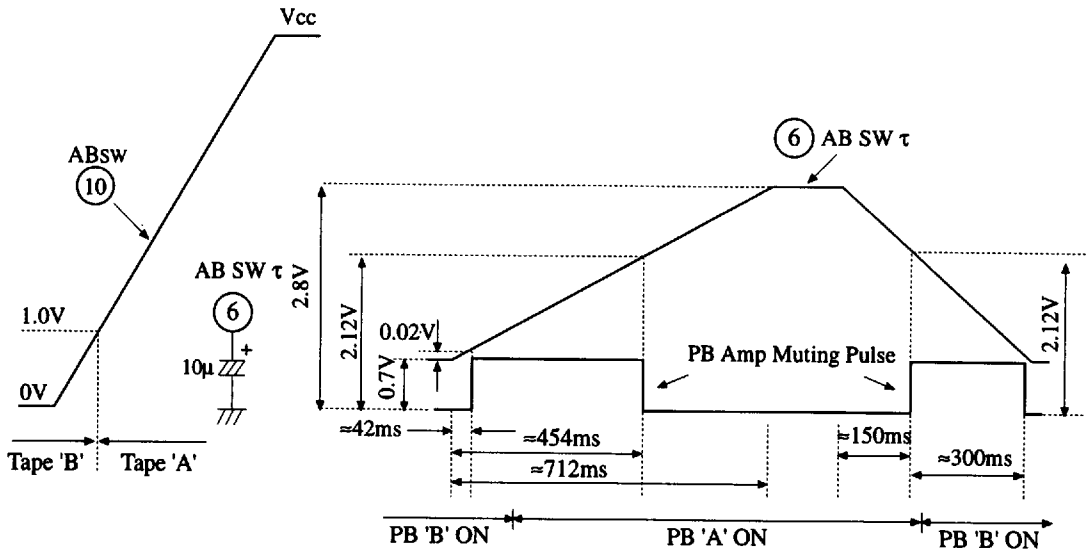


During dubbing mode, Sw1 will be in Rec position and point X will be bias at 2.1V internally ( $V_{cc} = 6V$ ). This is to ensure enough dynamic swing for the recording signal. Capacitor C is therefore necessary to couple the dc bias at point X to Rec bias oscillator. When in playback mode, point X will return to 0V and Sw1 is switch to PB position. Capacitor C should be chosen carefully to avoid degradation of the Rec bias Osc. signal & recording signal. The recommended value is  $22\mu F$ .

2) ALC Detector

The ALC circuit will be cut off during playback mode. This is achieved internally in the IC by shorting pin 16 to ground. By choosing different values of R, C combination at pin 16, the ALC attack and release time can be varied.

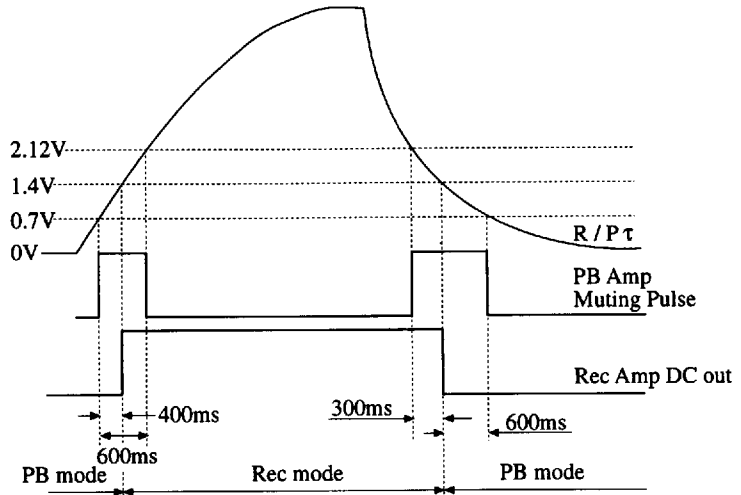
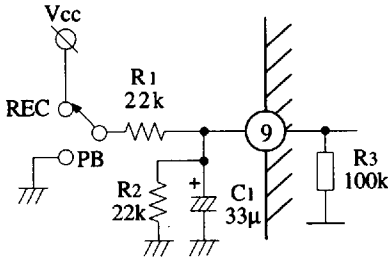
3) A/B Switch muting





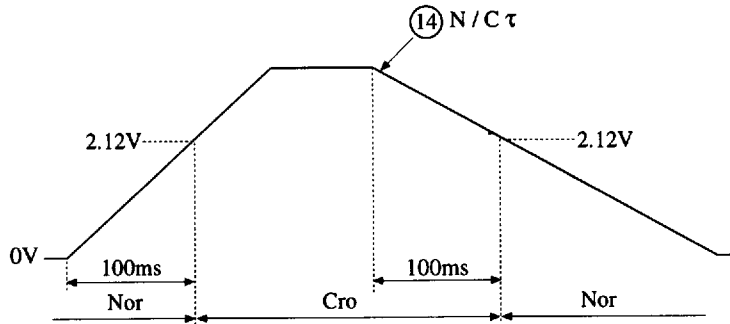
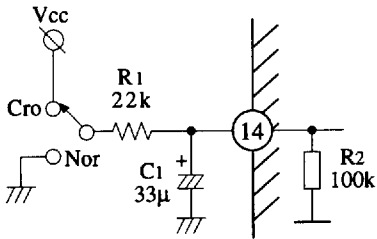
■ Supplementary Explanation (Continue)

4) R / PB Switching muting  
(A/B sw = 'B' mode)



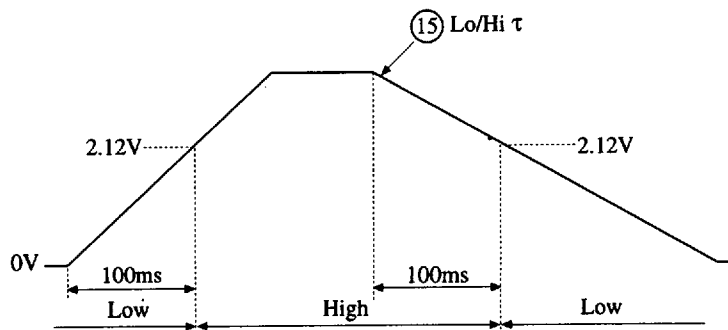
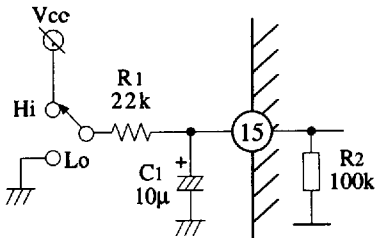
Charging  $\tau \approx R1 * C1$   
Discharging  $\tau \approx (R2 // R3) * C1$   
 $0.7V > \text{Threshold Voltage} > 2.1V$

5) Nor / Cro Switching



Charging  $\tau \approx R1 * C1$   
Discharging  $\tau \approx (R1 // R2) * C1$

6) Io / Hi Dubbing Switching

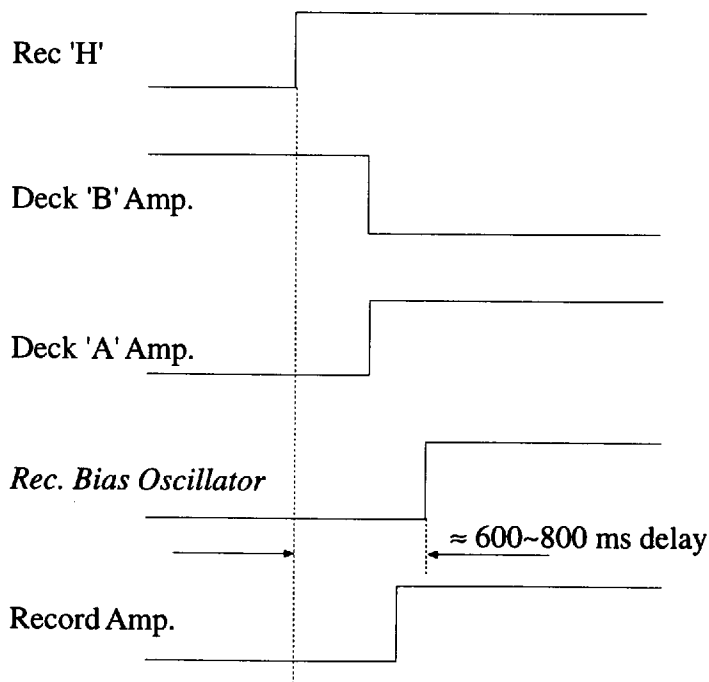


Charging  $\tau \approx R1 * C1$   
Discharging  $\tau \approx (R1 // R2) * C1$

■ Supplementary Explanation (Continue)

7) Rec 'H' swiching

When the Rec/PB switch (pin 9) is switched to record mode, the pre-amp will switch from deck 'B' to deck 'A' mode (if the ABsw, pin 10 is low). The pre-amp switching  $\tau$  is govern by the capacitor at pin 6. Therefore it is necessary to delay the turning ON time of the record bias oscillator circuit. This is to prevent any switching noise from the oscillator circuit from leaking through the 'B' amp during the initial switching period. The prefer switching sequence is shown below.



8) PCB layout for Pre -amp INPUTs.

To prevent oscillation, the input paths for pin 1 & 2 should avoid crossing or running next to the input paths for pin 23 & 24. This will also ensure minimum source leakage especially during record mode.

■ Printed Circuit Board Layout (Scale 1:1)

