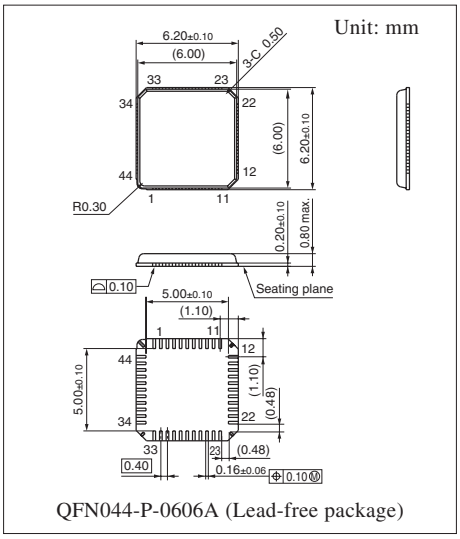
AN6591FJM

Transmission / reception, single chip PLL IC for PHS, cordless telephone

■ Overview

AN6591FJM is a single chip IC optimum for PHS, and a quadrature modulator, reception IF and PLL are integrated in it.

As this IC is housed in a QFN package (quad flat non-leaded PKG), realization of compact equipment through this super-small package is possible.



QFN044-P-0606A (Lead-free package)

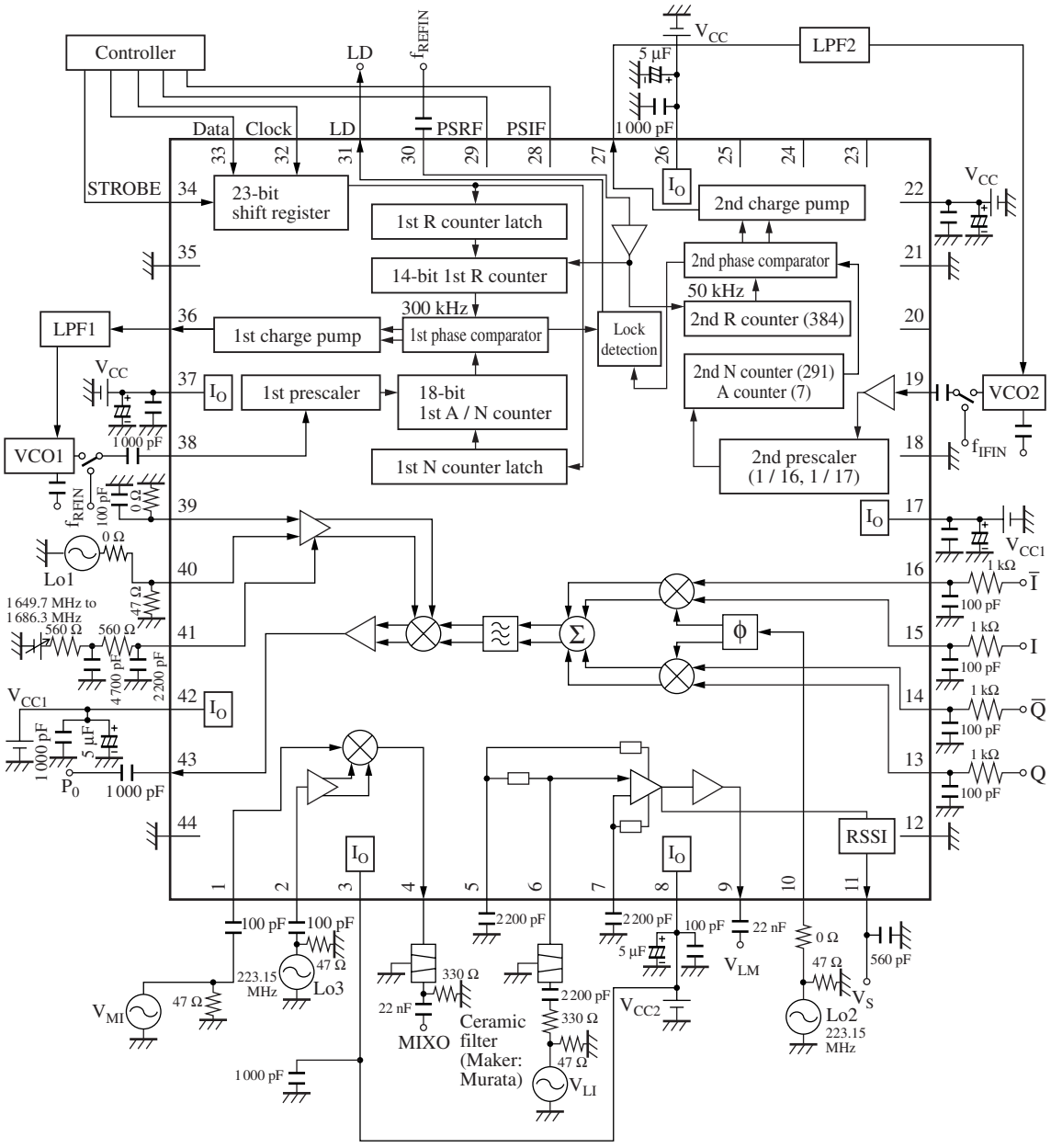
■ Features

- Transmission and reception PLL block on a single chip
- Transmission block: A quadrature modulator, a phase shifter APC (auto power control) and an up-converter
- Reception block: A down-mixer (to 300 MHz), an IF amplifier and an RSSI circuit
- PLL block: PLLs for 1st and 2nd local oscillators.
- 6 mm × 6 mm small package

■ Applications

- PHS, digital cordless telephone, etc.

■ Application Circuit Example



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	RXMXIN	RX mix. in	23	N.C.	—
2	RXLOIN	RX local in	24	N.C.	—
3	V_{CC2}	V_{CC} mix.	25	N.C.	—
4	MXO	Mix. out	26	V_{CC}	V_{CC} 2nd CMOS
5	LMDEC1	Lim. decouple1	27	CP2	2nd charge pump out
6	LMIN	Lim. in	28	PSIF	2nd power save in
7	LMDEC2	Lim. decouple2	29	PSRF	1st power save in
8	V_{CC2}	V_{CC} lim.	30	Ref.	Reference in
9	LMO	Lim. out	31	LD	Lock detect out
10	TXLO2	TX local2 in	32	Clock	Clock in
11	RSO	RSSI out	33	Data	Serial data in
12	GND	GND	34	STROBE	Strobe in
13	Q-in	Q-input	35	GND	GND 1st / 2nd CMOS
14	$\overline{Q}$-in	$\overline{Q}$-input	36	CP1	1st charge pump out
15	I-in	I-input	37	V_{CC}	V_{CC} 1st CMOS
16	$\overline{I}$-in	$\overline{I}$-input	38	RFIN	1st prescaler in
17	V_{CC1}	V_{CC} TX mod.	39	TXLO1	TX local 1
18	GNDM	GND TX mod.	40	TXLO1R	TX local 1ref.
19	IFIN	2nd prescaler in	41	APC / BS	APC / BS
20	N.C.	—	42	V_{CC1}	V_{CC} TX out
21	GND2	GND 2nd CMOS	43	TXO	TX output
22	V_{CC}	V_{CC} 1st 2nd BIP	44	GNDO	GND TX out

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC} V_{CC1} V_{CC2}	3.5	V
Supply current *2	I_{CC}	54	mA
Power dissipation *2	P_D	194	mW
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

*2: The above power dissipation P_D shows the power dissipation of the package without heat sink. Refer to "■ Technical Data" when mounting this IC to a PCB and check that the IC will operate within the package power dissipation range.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}, V_{CC1}, V_{CC2}	2.7 to 3.3	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Test circuit	Conditions	Min	Typ	Max	Unit
Current consumption (reception)	I_{CCRX}	2	No signal input	—	5.3	6.8	mA
Mix. conversion gain	G_{MX}	1	V_{MI} = 70 dBμ Filter loss excluded.	13	16	19	dB
Mix. max. output level	V_{MX}	1	V_{MI} = 105 dBμ Filter loss excluded.	105	110	—	dBμ
Lim. voltage gain	G_{LM}	1	V_{MI} = 20 dBμ	63	68	73	dB
Lim. max. output amplitude	V_{LM}	1	V_{LI} = 80 dBμ	350	400	—	mV[p-p]
RSSI output voltage (1)	V_S (1)	1	V_{LI}: No signal input	0	0.2	0.5	V
RSSI output voltage (2)	V_S (2)	1	V_{LI} = 115 dBμ	1.60	1.80	—	V
Change in RSSI output	D_S	1	V_S (V_{IS}) = V_S(1) + 0.15 V D_S (1) = V_S (V_{IS} + 65 dBμ) − V_S (V_{IS})	1.0	1.25	1.5	V
Gradient of RSSI output	$\Delta D_{S(n)}$	1	ΔD_S (n) = 5 (V_S (V_{IS} + n13 dBμ) − V_S (V_{IS} + (n − 1) 13 dBμ)) / D_S (1) n = 1 to 5	0.75	1.0	1.25	—
Current consumption (transmission)	I_{CCTX}	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V	—	28	37	mA
Sleep current in transmission	ISL	2	No signal input, V_{APC} = 0 V	—	0	10	μA
Transmission output level 1 *	P01	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 660 MHz, −10 dBm, V_{APC} = 2.2 V	−13	−9	—	dBm
Transmission output level 2 *	P02	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 687 MHz, −10 dBm, V_{APC} = 2.2 V	−13	−9	—	dBm
Image leakage suppression	IL1	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V, I / Q: No level adjusted	—	−35	−30	dBc
$f_{LO1} + f_{LO2}$ leakage suppression	CL	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V, I / Q: DC offset adjusted	—	−35	−30	dBc
Proximity spurious suppression	DU	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm Make V_{APC} adjustments so that the Po value will be −13 dBm.	—	−55	−51	dBc

Note) 1. Unless otherwise specified, at reception: V_{CC2} = 3.0 V, V_{LO3} = −10 dBm, f = 233.15 MHz, V_{MI}: f = 243.95 MHz, SW1 = a, V_{LI}: f = 10.8 MHz (The input level of pin 6, except the signal attenuation at the matching circuit and filter circuit.)
The V_{MO} and V_{LO} values are at high impedance. (V_{LM} shall be measured at probe load conditions of 27 pF and 1 MΩ.)

2. The V_{IS} is the input level V_{LI} where the RSSI output voltage is V_S (1) + 0.15 V. At transmission: V_{CC1} = 3.0 V, I / Q signal amplitude: 0.5 V[p-p] in both phases, DC bias: 1.5 V, SW1: a
I_{CCTX} , IL1, CL: π / 4 QPSK-modulated wave, P01, P02, DU: PN9-level-modulated wave
I / Q signal input condition: Make an amplitude adjustment of π / 4 QPSK modulation signal 0000 to 0.5 V[p-p] with an oscilloscope and change the signal wave to a PN9-level continuous wave.
Spectrum analyzer setting conditions for transmission output level measurement: SPAN = 2 MHz, RBW = 3 MHz, VBW = 3 MHz, SWPT = 5 s Det.: Pose. peak

*: P01 output frequency: 1 893.15 MHz, P02 output frequency: 1 920.15 MHz

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Test circuit	Conditions	Min	Typ	Max	Unit
Current consumption 1 (PLL)	I_{CC1}	1	1st PLL and 2nd PLL blocks are simultaneously turned on.	3.7	5.4	7.0	mA
Current consumption 2 (PLL)	I_{CC2}	1	1st PLL block is turned on while the 2nd PLL block is turned off.	3.0	4.4	5.7	mA
Current consumption 3 (PLL)	I_{CC3}	1	1st PLL block is turned off while the 2nd PLL block is turned on.	1.2	1.7	2.2	mA
Current consumption 4 (PLL)	I_{CC4}	1	Power save mode	—	0	10	µA
1st RF input level	V_{RFIN}	1	f_{RFIN} = 1 500 MHz to 1 800 MHz	−15	—	−2	dBm
2nd IF input level	V_{IFIN}	1	f_{IFIN} = 120 MHz to 300 MHz	−10	—	+6	dBm
Reference signal input level	V_{REFIN}	1	f_{REFIN} = 10 MHz to 25 MHz	0.2	—	1.2	V[p-p]

Note) Unless otherwise specified, V_{CC} is 3.0 V and reference signal input level V_{REFIN} is 0.6 V[p-p] at f_{REFIN} = 19.2 MHz.

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Test circuit	Conditions	Min	Typ	Max	Unit
1st local leakage suppression	CL1	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V	—	−25	−20	dBc
2nd local leakage suppression	CL2	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V	—	−15	−10	dBc
In-band output level deviation	$\lvert\Delta P\rvert$	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 660 MHz to 1 687 MHz, −10 dBm, V_{APC} = 2.2 V	—	—	1.0	dB
Adjacent channel leakage power suppression (600 kHz detuning)	BL1	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V	—	−60	—	dBc
Modulation accuracy	EVM	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.2 V	—	3	5	%[rms]
Min. output level	Pmin	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 1.0 V	—	−30	−25	dBm
RF + 233.15 MHz leakage suppression	IIL	1	Lo1 = 233.15 MHz, −10 dBm Lo2 = 1 672.5 MHz, −10 dBm V_{APC} = 2.75 V	—	−36	—	dBc
Mixer output resistance	Rmix	2	No signal input	—	330	—	Ω

Note) Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2}$ = 3.0 V
I / Q signal: 0.5 V[p-p] in both phases, DC bias: 1.5 V
CL1, CL2, $\lvert\Delta P\rvert$, BL1, EVM, Pmin, IIL : PN9-level modulated wave.

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Test circuit	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2		2.4	—	—	V
Low-level input voltage	V_{IL}	2		—	—	0.6	V
High-level output voltage	V_{OH}	2		2.4	—	—	V
Low-level output voltage	V_{OL}	2		—	—	0.6	V
High-level input current 1	I_{IH1}	2	V_{IH} of 3.0 V applied	—	0	10	µA
Low-level input current 1	I_{IL1}	2	V_{IL} of 0 V applied	—	0	10	µA
High-level input current 2	I_{IH2}	2	V_{IH} of 3.0 V applied	—	0	10	µA
Low-level input current 2	I_{IL2}	2	V_{IL} of 0 V applied	—	0	10	µA
High-level output current 1 / 2 (High power)	$I_{OH1H,2H}$	2	High power with V_{OH} of 2.4 V applied.	−3.2	−2.6	−1.9	mA
Low-level output current 1 / 2 (High power)	$I_{OL1H,2H}$	2	High power with V_{OL} of 0.6 V applied.	2.8	3.5	4.4	mA
High-level output current 1 / 2 (Low power)	$I_{OH1L,2L}$	2	Low power with V_{OH} of 2.4 V applied.	− 0.74	− 0.6	− 0.46	mA
Low-level output current 1 / 2 (Low power)	$I_{OL1L,2L}$	2	Low power with V_{OL} of 0.6 V applied.	0.53	0.7	0.87	mA
Output leakage current	I_{OZ}	2	V_{OZ} of 0 V / 3.0 V applied	−1	0	1	µA
High-level output current 3	I_{OH3L}	2	V_{OH} of 2.4 V applied	−3.6	−2.6	−1.5	mA
Low-level output current 3	I_{OL3L}	2	V_{OL} of 0.6 V applied	1.9	3.3	4.6	mA
Lockup time (1st)	rockt1	1	1st PLL block and 2nd PLL block are simultaneously turned on for all channels with RX-to-TX and TX-to-RX burst.	—	—	600	µs
Lockup time (2nd)	rockt2	1	1st PLL block and 2nd PLL block are simultaneously turned on intermittently (during PS triggering)	—	—	600	µs
1st spurious ±50 kHz	Lspu1	1	1st PLL block and 2nd PLL block are simultaneously turned on. L-channel to H-channel	—	—	−40	dBc
1st proximity C / N	Lspu2	1	1st PLL block and 2nd PLL block are simultaneously turned on. df = 1 kHz, L-channel to H-channel	—	—	−70	dBc / Hz
1st reference leakage	Lspu3	1	1st PLL block and 2nd PLL block are simultaneously turned on. df = 600 kHz, BW192 kHz	—	—	−67	dBc

Note) Unless otherwise specified, V_{CC} is 3.0 V and reference signal input level V_{REFIN} is 0.6 V[p-p] at f_{REFIN} of 19.2 MHz.

■ Electrical Characteristics at T_a = 25°C (continued)

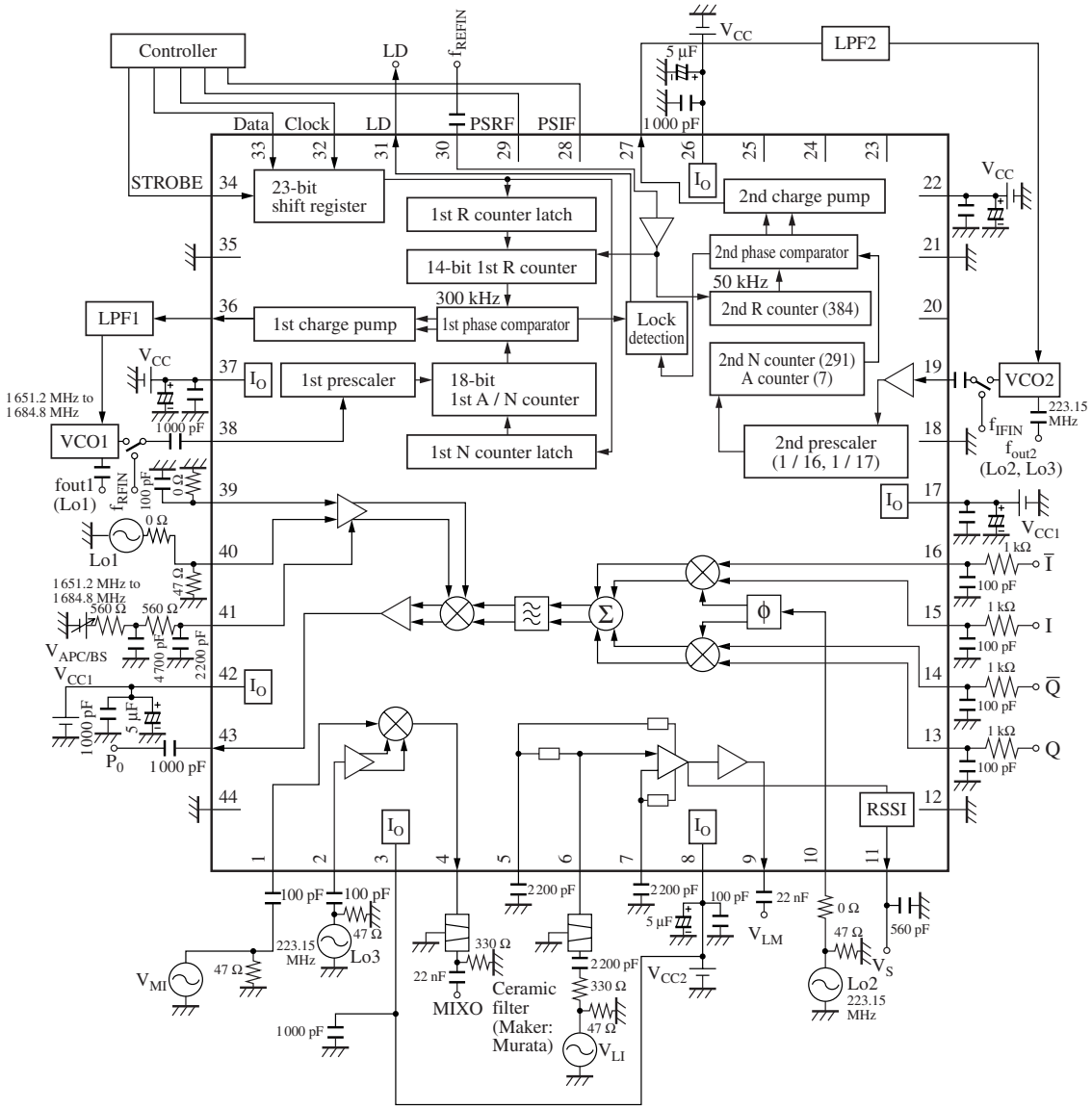
• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Test circuit	Conditions	Min	Typ	Max	Unit
2nd reference leakage ±50 kHz	Lspu4	1	1st PLL block and 2nd PLL block are simultaneously turned on. RW 1 kHz, VW 1 kHz	—	—	–40	dBc
2nd proximity C / N	Lspu5	1	1st PLL block and 2nd PLL block are simultaneously turned on. df = 1 kHz	—	—	–76	dBc / Hz

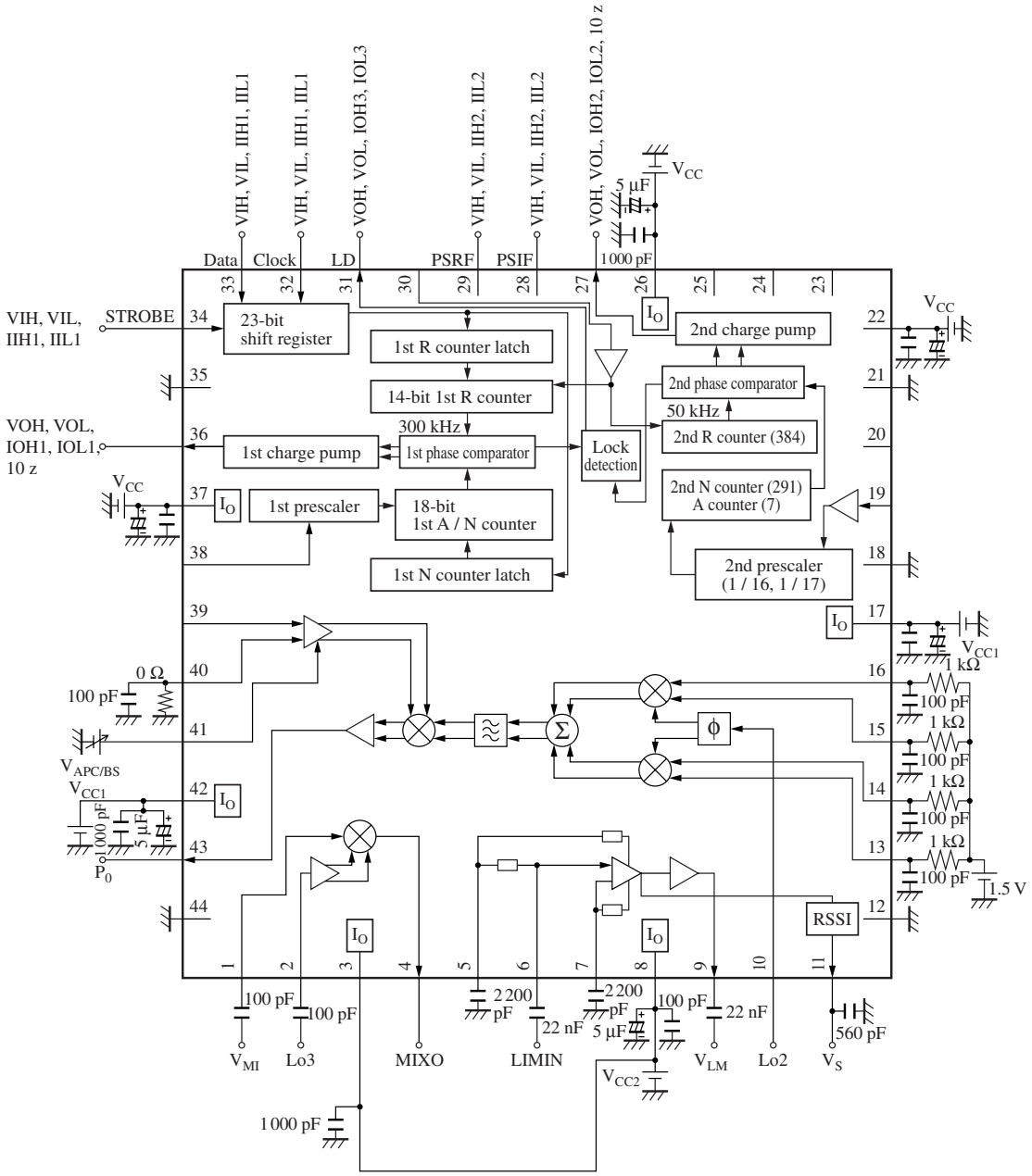
Note) Unless otherwise specified, V_{CC} is 3.0 V and reference signal input level V_{REFIN} is 0.6 V[p-p] at f_{REFIN} of 19.2 MHz.

1. Test circuit 1

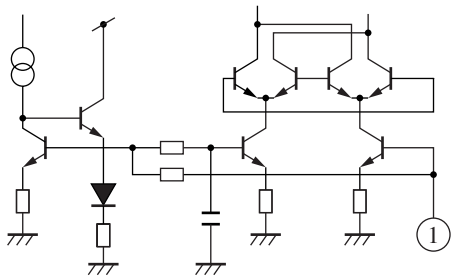
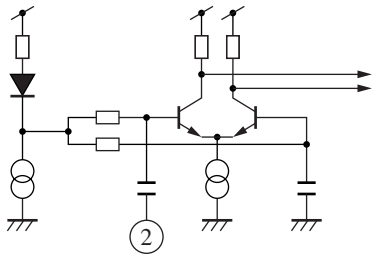
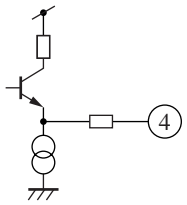
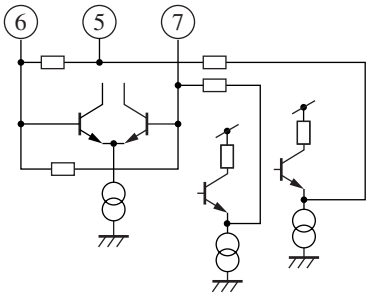
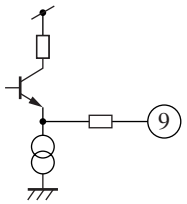


■ Electrical Characteristics at T_a = 25°C (continued)

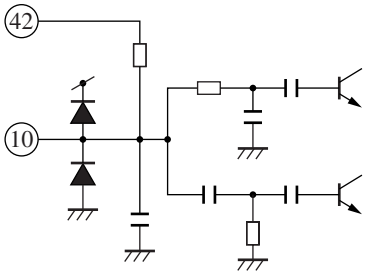
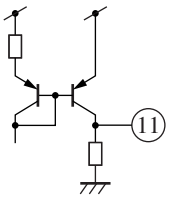
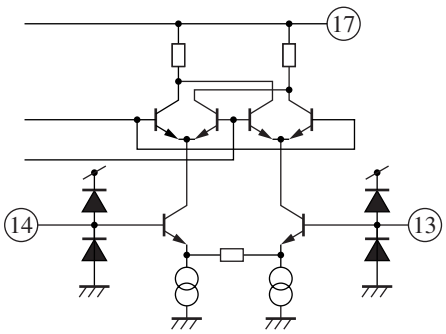
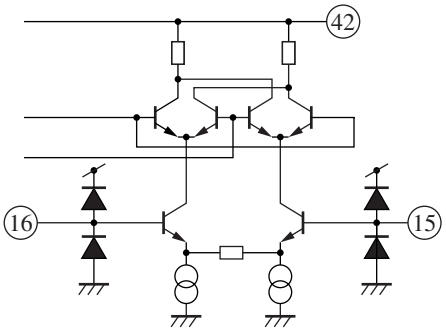
2. Test circuit 2



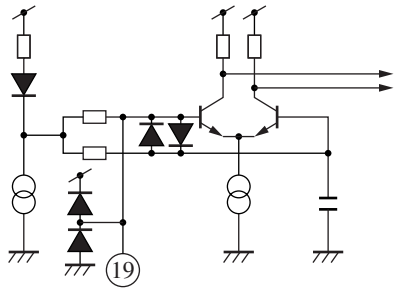
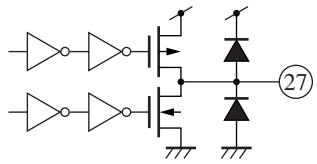
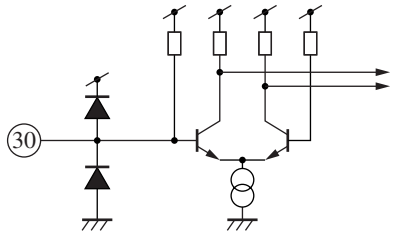
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I / O
1		RXMIXIN: Reception mixer input pin with an input impedance of approx. 16 kΩ.	I
2		RXLOIN: Local input pin.	I
3	—	V_{CC2}: Mixer power supply pin.	—
4		MXO: Mixer output pin.	O
5		LMDEC1, 2: Coupling pin for limiter amplifier feedback. Ground this pin through an external capacitor.	—
7			
6		LMIN: Limiter amplifier input pin with an input impedance of approx. 330 Ω.	I
8	—	V_{CC2}: Pin to provide power supply to the limiter amplifier and RSSI.	—
9		LMO: Limiter amplifier output pin.	O

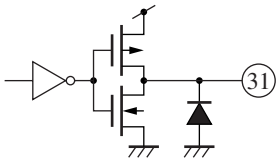
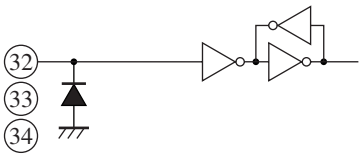
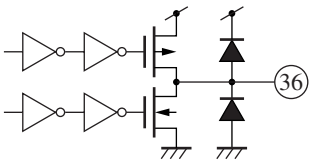
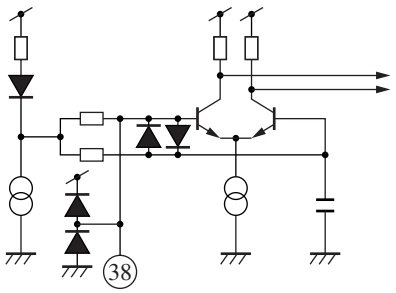
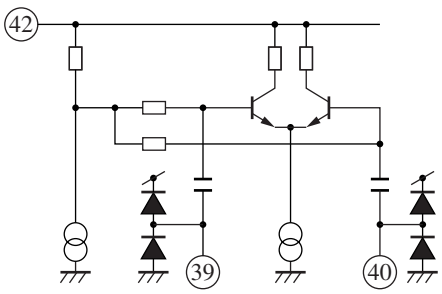
■ Terminal Equivalent Circuits (continued)

<table>
<tr><th>Pin No.</th><th>Equivalent circuit</th><th>Description</th><th>I / O</th></tr>
<tr><td>10</td><td> 
</td><td>TXLO2:
Quadrature modulator local input pin</td><td>I</td></tr>
<tr><td>11</td><td> 
</td><td>RSO:
RSSI output pin with DC output according to the input signal level of the limiter amplifier.</td><td>O</td></tr>
<tr><td>12</td><td>—</td><td>GNDR: Ground pin.</td><td>—</td></tr>
<tr><td>13</td><td rowspan="2"> 
</td><td>Q-in:
Q signal input pin with the following relationship between the input DC bias and amplitude.<table><tr><th>DC bias (V)</th><th>Amplitude V[p-p]</th></tr><tr><td>1.5</td><td>0.5 (Both phases)</td></tr></table></td><td>I</td></tr>
<tr><td>14</td><td>$\overline{Q}$-in:
$\overline{Q}$ signal input pin with the following relationship between the input DC bias and amplitude.<table><tr><th>DC bias (V)</th><th>Amplitude V[p-p]</th></tr><tr><td>1.5</td><td>0.5 (Both phases)</td></tr></table></td><td>I</td></tr>
<tr><td>15</td><td rowspan="2"> 
</td><td>I-in:
I signal input pin with the following relationship between the input DC bias and amplitude.<table><tr><th>DC bias (V)</th><th>Amplitude V[p-p]</th></tr><tr><td>1.5</td><td>0.5 (Both phases)</td></tr></table></td><td>I</td></tr>
<tr><td>16</td><td>$\overline{I}$-in:
$\overline{I}$ signal input pin with the following relationship between the input DC bias and amplitude.<table><tr><th>DC bias (V)</th><th>Amplitude V[p-p]</th></tr><tr><td>1.5</td><td>0.5 (Both phases)</td></tr></table></td><td>I</td></tr>
</table>

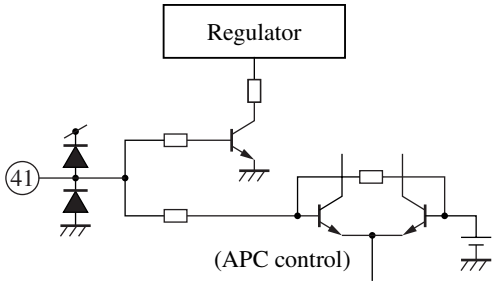
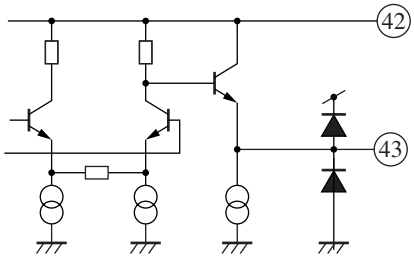
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I / O
17	—	V_{CC1}: Pin to provide supply voltage to the quadrature modulator. The pin is connected to the built-in band gap regulator, thus providing stable bias voltage without being affected by V_{CC} or temperature changes as much as possible.	I
18	—	GNDM: Ground pin for the quadrature modulator. Keep the grounding surface wide to lower the impedance.	—
19		2nd prescaler in: 2nd PLL prescaler input pin.	I
21	—	GND 2nd CMOS: Ground pin for the 2nd PLL.	—
22	—	V_{CC}: Bip power supply pin for the PLL.	—
26	—	V_{CC}: 2nd CMOS power supply pin for the PLL.	—
27		2nd chargepump out: 2nd PLL charge pump output pin.	O
28 29		28: 2nd power save in: 29: 1st power save in: 2nd PLL and 1st PLL power save control input pins.	I
30		Reference in: Reference signal input pin.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I / O
31		Lock detect out: Lock detection output pin.	O
32 33 34		32: Clock in: Clock input pin. 33: Serial data in: Data input pin. 34: Strobe in: Strobe input pin.	I
35	—	GND 1st / 2nd CMOS: 1st and 2nd PLL ground pin.	—
36		1st charge pump out: 1st PLL charge pump output pin.	O
37	—	V_{CC}: 1st PLL CMOS power supply pin.	—
38		1st prescaler in: 1st PLL prescaler input pin.	I
39		TX LO1: Local input pin for the up-mixer. The use of an external balancer is recommended to apply balanced input.	I
40		TX LO1R: Local input pin for the up-mixer. The use of an external balancer is recommended to apply balanced input.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I / O
41		APC / BS: Pin used for the battery save of the transmission circuit block and the power control of RF output. V_{APC} (V) / Status: 0 to 0.3 / Off; 1.0 to V_{CC} / On (APC control) The impedance is a minimum of 5 kΩ.	I
42	—	V_{CC1}: Pin to provide power supply to the up-mixer and output amplifier circuit. This pin is connected to the built-in stabilized power supply circuit and provides stable bias voltage without being affected by V_{CC} or temperature changes as much as possible.	—
43		TXO: RF output pin connected to the output amplifier circuit and has emitter follower output.	O
44	—	GNDO: Ground pin for the up-mixer and output amplifier circuit. This pin is a high-frequency ground pin. Therefore, keep the grounding surface wide to lower the impedance.	—

■ Technical Data

1. Serial data interface specifications

Carrier data is transferred in 23-bit serial data transfer. The serial data is set at the clock falling edge and latched onto the synthesizer at the clock rising edge. It is necessary to input a single STROBE pulse when the 23-bit serial data transfer is completed.

1) Serial interface of 1st synthesizer

1st synthesizer serial data input format

MSB LSB

N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	A6	A5	A4	A3	A2	A1	A0	PD	P	TC	C1	C0
X	X	X	TO	X	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	T1	T0	C1	C0

←N data input direction X: don't care

$f_{out} = (P \times N + A) \times f_{in} / R$

Possible set range: 1st A = 0 to 127 or 63, N = 5 to 2047 (N > A)
R = 5 to 16383

(1) Control bit

C0	C1	
1	0	1st synthesizer R counter frequency dividing ratio setting
1	1	1st synthesizer A / N counter frequency dividing ratio setting

(2) Test contents

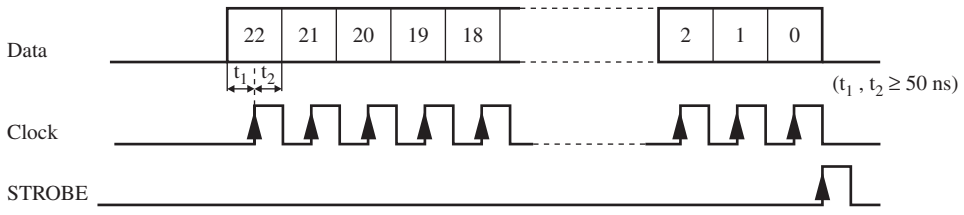
	T0	T1
2nd synthesizer R counter output	0	0
2nd synthesizer N counter output	0	1
1st synthesizer R counter output	1	0
1st synthesizer N counter output	1	1

(3) Data contents

	PD Phase comparator polarity selection	P Prescaler frequency dividing ratio	TC Counter test mode setting	TO Output pin test
0	negative	128 / 129	LD output	normal
1	positive	64 / 65	Counter output	test

2) Serial transfer timing

Timing chart



■ Technical Data (continued)

2. 2nd synthesizer frequency dividing ratio

Set frequency (frequency dividing ratio) f_{out2} = 233.15 MHz, f_r = 50 kHz, (P = 16, N = 291, A = 7, R = 384 fixed)
Reference frequency f_{REFIN} = 19.2 MHz

MSB LSB

N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	X	X	X	A3	A2	A1	A0	PD	P	X
0	0	1	0	0	1	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0

X	X	X	X	X	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	X	X
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

X: don't care

3. Unlock detection and LD output specifications

1) The AND of the LD signal (2) of the 1st synthesizer block and the LD signal (3) of the 2nd synthesizer block is output.
2) 1st synthesizer block

When the synthesizer block is locked, the LD output level will be high. When the synthesizer block is unlocked, the LD output level will be low. The detection time is 3.3 µs. As for the precision of detection, unlock output turns on if the devided frequency output of the circuit is (52 × 4) ns slower or faster than it should be at the frequency f_{ref} of 300 kHz. The lock signal is output in power save mode.

3) 2nd synthesizer block

When the synthesizer block is locked, the LD output level will be high. When the synthesizer block is unlocked, the LD output level will be low. The detection time is 20 µs. As for the precision of detection, unlock output turns on if the devided frequency output of the circuit is (52 × 4) ns slower or faster than it should be at the frequency f_{ref} of 50 kHz. The lock signal is output in power save mode.

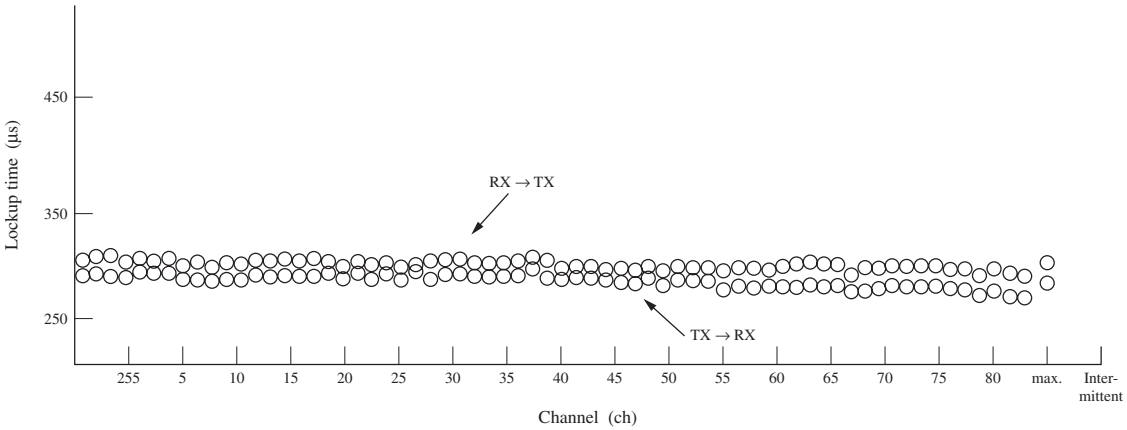
1st synthesizer	2nd synthesizer	LD output
Lock or power save mode	Lock or power save mode	High
Unlock	Lock or power save mode	Low
Lock or power save mode	Unlock	Low
Unlock	Unlock	Low

4. Other specifications

1) Clock, Data, and STROBE all are high-active logics.
2) When the IC is turned on, set the IC to power save mode by setting both PS1 and PS2 to low-level. After serial data is input, set the IC to operating mode by setting both PS1 and PS2 to high-level.

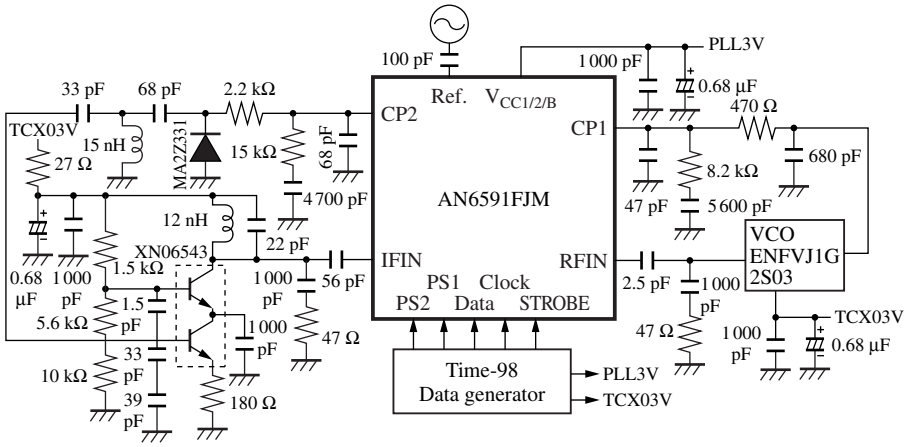
■ Technical Data (continued)

3. TX-RX burst / intermittent reception lockup time



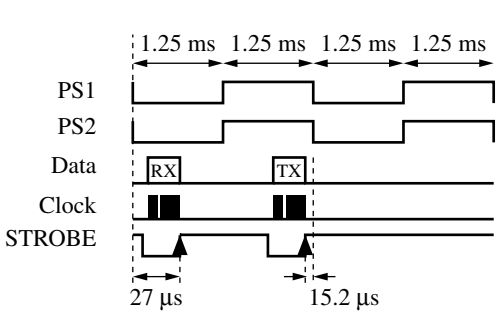
Unless otherwise specified, V_{CC} = 3.0 V, and f_{REF} = 19.2 MHz.
The lockup time means converging time into ±1 kHz.

1) Test circuit

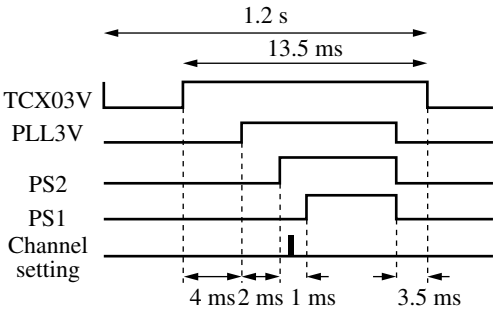


2) Serial control timing

(1) At TX-RX burst



(2) At intermittent reception



■ Technical Data (continued)

4. Oscillator frequency by channel (f_{RFIN})

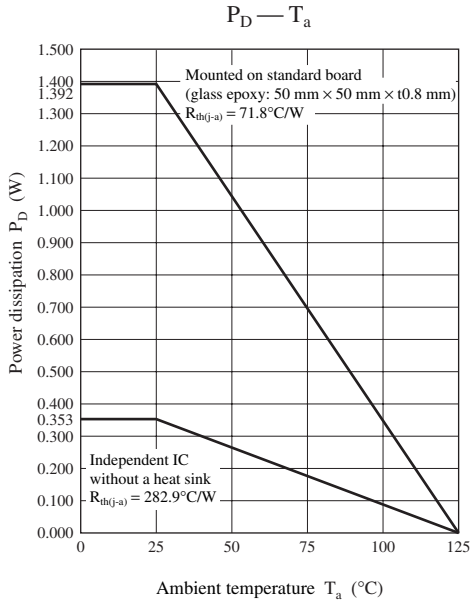
ch	f_{RFIN} <TX> (MHz)	f_{RFIN} <RX> (MHz)	ch	f_{RFIN} <TX> (MHz)	f_{RFIN} <RX> (MHz)
251	1660.5	1649.7	31	1671.0	1660.2
252	1660.8	1650.0	32	1671.3	1660.5
253	1666.1	1650.3	33	1671.6	1660.8
254	1666.4	1650.6	34	1671.9	1661.1
255	1666.7	1650.9	35	1672.2	1661.4
1	1662.0	1651.2	36	1672.5	1661.7
2	1662.3	1651.5	37	1672.8	1662.0
3	1662.6	1651.8	38	1673.1	1662.3
4	1662.9	1652.1	39	1673.4	1662.6
5	1663.2	1652.4	40	1673.7	1662.9
6	1663.5	1652.7	41	1674.0	1663.2
7	1663.8	1653.0	42	1674.3	1663.5
8	1664.1	1653.3	43	1674.6	1663.8
9	1664.4	1653.6	44	1674.9	1664.1
10	1664.7	1653.9	45	1675.2	1664.4
11	1665.0	1654.2	46	1675.5	1664.7
12	1665.3	1654.5	47	1675.8	1665.0
13	1665.6	1654.8	48	1676.1	1665.3
14	1665.9	1655.1	49	1676.4	1665.6
15	1666.2	1655.4	50	1676.7	1665.9
16	1666.5	1655.7	51	1677.0	1666.2
17	1666.8	1656.0	52	1677.3	1666.5
18	1667.1	1656.3	53	1677.6	1666.8
19	1667.4	1656.6	54	1677.9	1667.1
20	1667.7	1656.9	55	1678.2	1667.4
21	1668.0	1657.2	56	1678.5	1667.7
22	1668.3	1657.5	57	1678.8	1668.0
23	1668.6	1657.8	58	1679.1	1668.3
24	1668.9	1658.1	59	1679.4	1668.6
25	1669.2	1658.4	60	1679.7	1668.9
26	1669.5	1658.7	61	1680.0	1669.2
27	1669.8	1659.0	62	1680.3	1669.5
28	1670.1	1659.3	63	1680.6	1669.8
29	1670.4	1659.6	64	1680.9	1670.1
30	1670.7	1659.9	65	1681.2	1670.4

■ Technical Data (continued)

4. Oscillator frequency by channel (f_{RFIN}) (continued)

ch	f_{RFIN} <TX> (MHz)	f_{RFIN} <RX> (MHz)	ch	f_{RFIN} <TX> (MHz)	f_{RFIN} <RX> (MHz)
66	1 681.5	1 670.7	77	1 684.8	1 674.0
67	1 681.8	1 671.0	78	1 685.1	1 674.3
68	1 682.1	1 671.3	79	1 685.4	1 674.6
69	1 682.4	1 671.6	80	1 685.7	1 674.9
70	1 682.7	1 671.9	81	1 686.0	1 675.2
71	1 683.0	1 672.2	82	1 686.3	1 675.5
72	1 683.3	1 672.5	max.	1 686.3	1 649.7
73	1 683.6	1 672.8		(1st)	(2nd)
74	1 683.9	1 673.1	Inter-	1 662.6	233.15
75	1 684.2	1 673.4	mittent		
76	1 684.5	1 673.7			

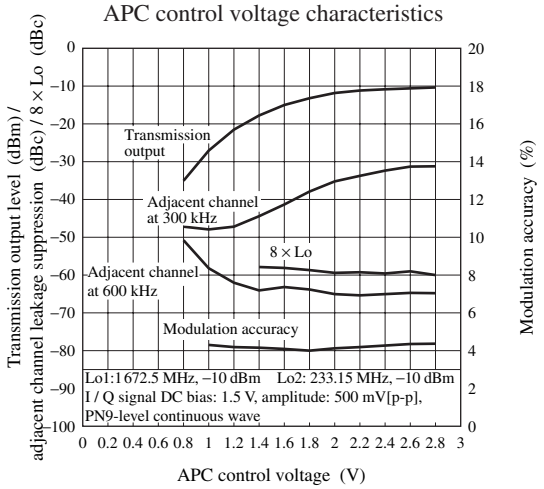
5. P_D — T_a curves of QFN044-P-0606A



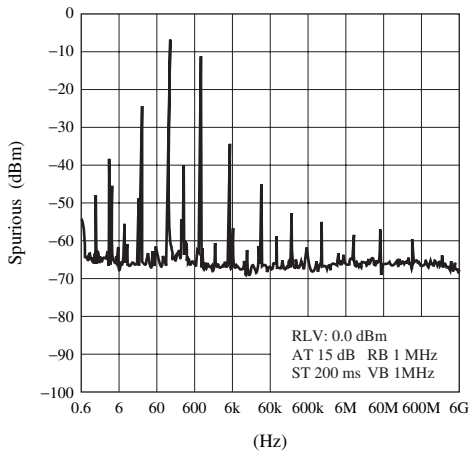
■ Technical Data (continued)

6. Main characteristics

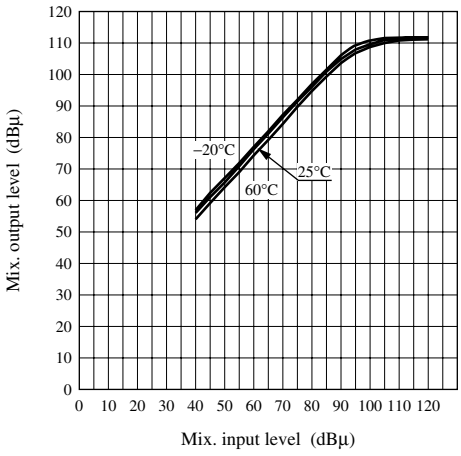
APC control voltage characteristics



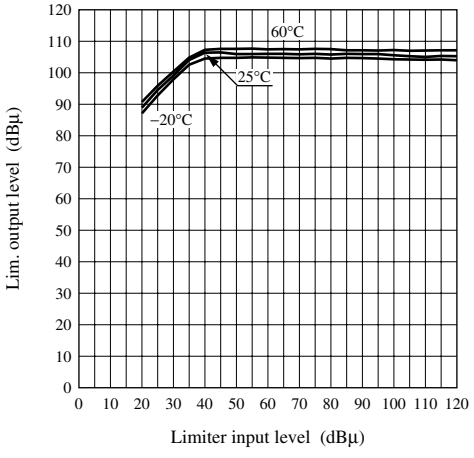
Wideband spurious characteristics



AN6591FJM Mix.I / O characteristics



AN6591FJM Lim. characteristics

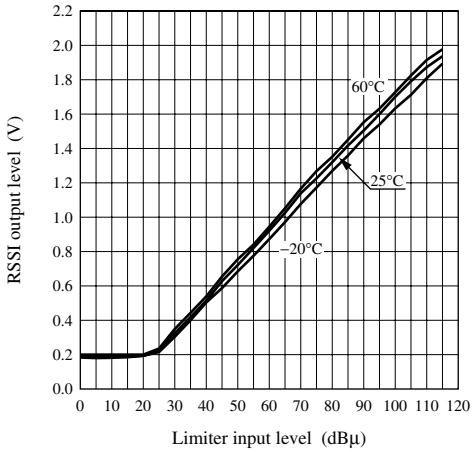


Note) 1. Unless otherwise specified, the test conditions conform to electrical characteristics.
2. The values in the above are reference values for designing and not guaranteed.

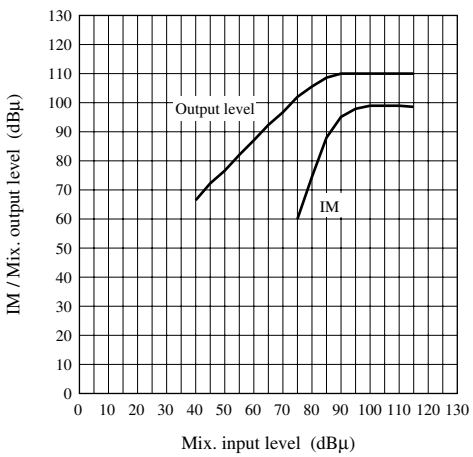
■ Technical Data (continued)

6. Main characteristics (continued)

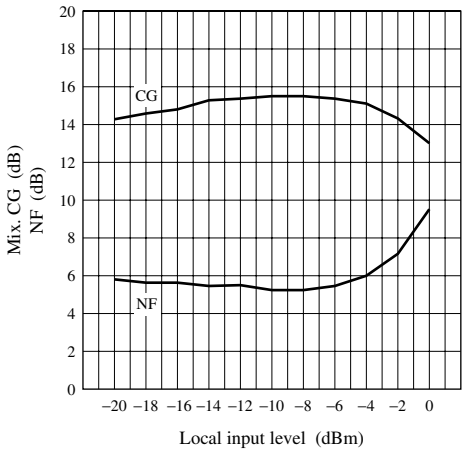
AN6591FJM RSSI characteristics



AN6591FJM Mix. characteristics



AN6591FJM Mix. characteristics



Note) 1. Unless otherwise specified, the test conditions conform to electrical characteristics.

2. The values in the above are reference values for designing and not guaranteed.

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