

74F64 4-2-3-2-Input AND-OR-Invert Gate

General Description

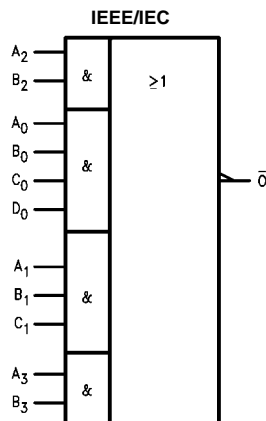
This device contains gates configured to perform a 4-2-3-2 input AND-OR-INVERT function.

Ordering Code:

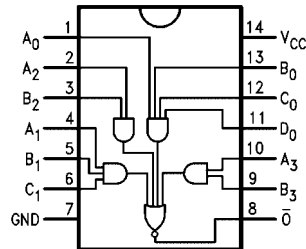
Order Number	Package Number	Package Description
74F64SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F64SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F64PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
A_n, B_n, C_n, D_n	Inputs	1.0/1.0	20 μ A/-0.6 mA
$\bar{0}$	Output	50/33.3	-1 mA/20 mA

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

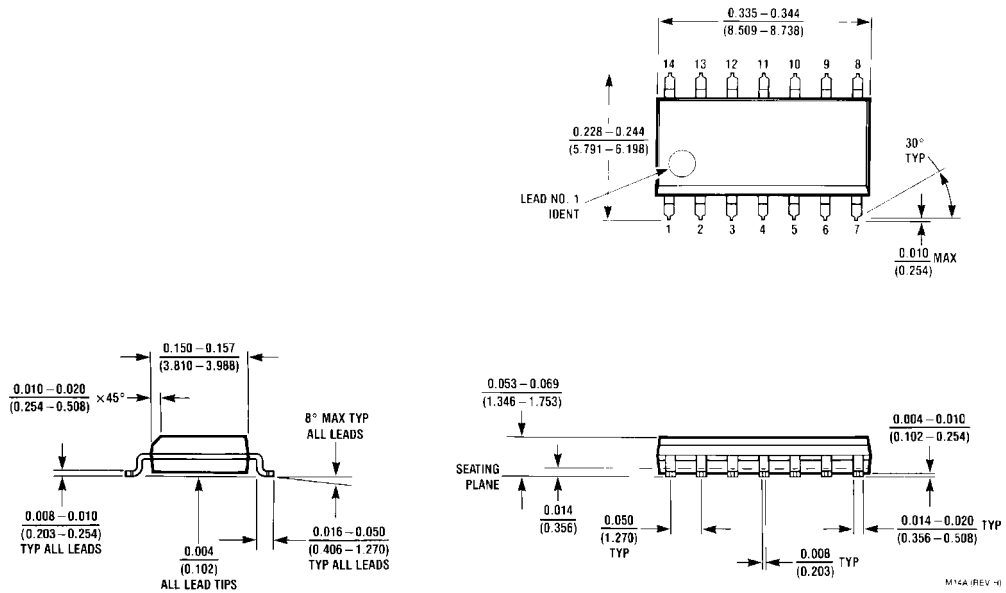
DC Electrical Characteristics

Symbol	Parameter	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	V	Min I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}	V	Min I _{OL} = 20 mA
I _{IH}	Input HIGH Current	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output High Leakage Current	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0° to +70°C C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	4.6	6.5	2.5	7.5	ns
t _{PHL}	A _n , B _n , C _n , D _n to \bar{O}	1.5	3.2	4.5	1.5	5.5	

Physical Dimensions inches (millimeters) unless otherwise noted



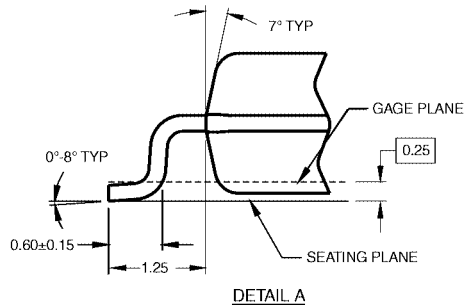
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



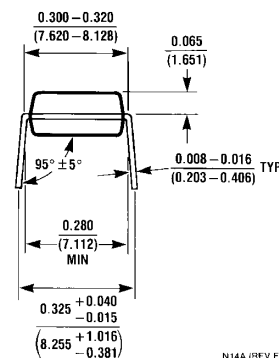
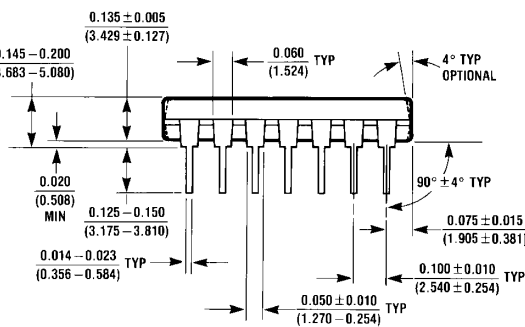
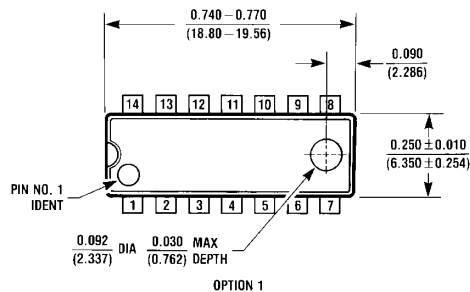
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

N14A (REV F)

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