

74F538 1-of-8 Decoder with 3-STATE Outputs

General Description

The 74F538 decoder/demultiplexer accepts three Address (A_0 - A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable (OE) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

Features

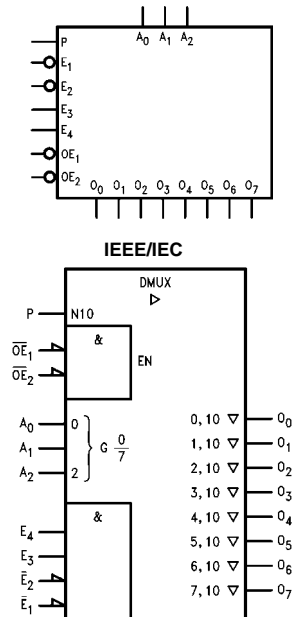
- Output polarity control
- Data demultiplexing capability
- Multiple enables for expansion
- 3-STATE outputs

Ordering Code:

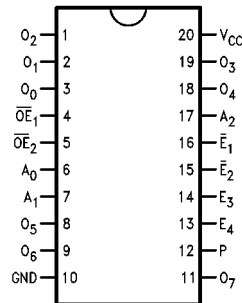
| Order Number | Package Number | Package Description |
|--------------|----------------|---------------------------------------------------------------------------|
| 74F538SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F538SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F538PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

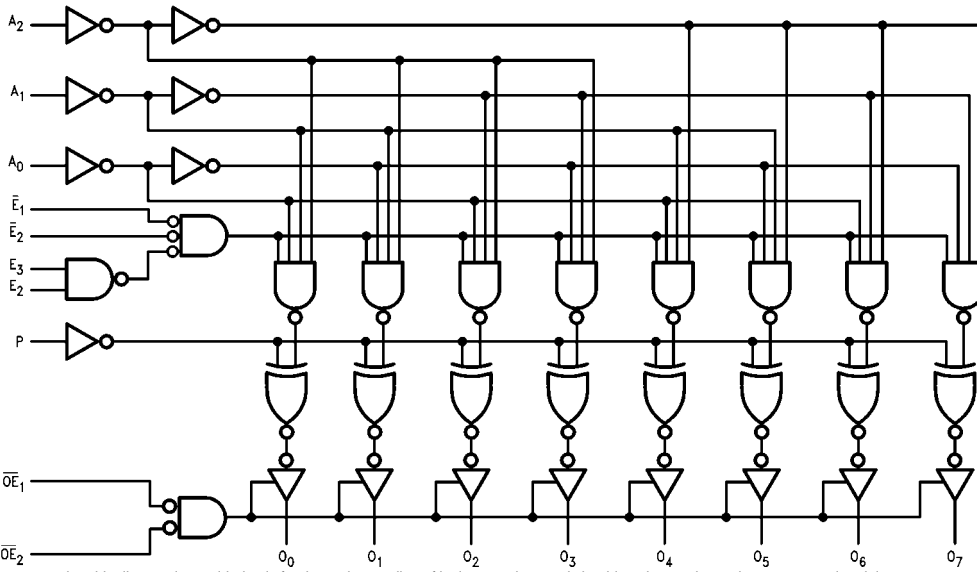
| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|------------------------------------|-----------------------------------|------------------|-------------------------------------------------|
| A_0 - A_2 | Address Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| $\overline{E}_1, \overline{E}_2$ | Enable Inputs (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| E_3, E_4 | Enable Inputs (Active HIGH) | 1.0/1.0 | 20 μ A/-0.6 mA |
| P | Polarity Control Input | 1.0/1.0 | 20 μ A/-0.6 mA |
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable Inputs (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| O_0 - O_7 | 3-STATE Outputs | 150/40 (33.3) | -3 mA/24 mA (20 mA) |

Truth Table

| Function | Inputs | | | | | | | | | Outputs | | | | | | | |
|----------------------------------|-------------------|-------------------|------------------|-------|-------|-------|-------|-------|-------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| | \overline{OE}_1 | \overline{OE}_2 | \overline{E}_1 | E_2 | E_3 | E_4 | A_2 | A_1 | A_0 | O_0 | O_1 | O_2 | O_3 | O_4 | O_5 | O_6 | O_7 |
| High | H | X | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z |
| Impedance | X | H | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z |
| Disable | L | L | H | X | X | X | X | X | X | Outputs Equal P Input | | | | | | | |
| | L | L | X | H | X | X | X | X | X | | | | | | | | |
| | L | L | X | X | L | X | X | X | X | | | | | | | | |
| | L | L | X | X | X | L | X | X | X | | | | | | | | |
| Active HIGH Output (P = L) | L | L | L | L | H | H | L | L | L | H | L | L | L | L | L | L | L |
| | L | L | L | L | H | H | L | L | H | L | H | L | L | L | L | L | L |
| | L | L | L | L | H | H | L | H | H | L | L | L | H | L | L | L | L |
| | L | L | L | L | H | H | H | L | L | L | L | L | L | H | L | L | L |
| | L | L | L | L | H | H | H | L | H | L | L | L | L | L | H | L | L |
| | L | L | L | L | H | H | H | H | L | L | L | L | L | L | L | H | L |
| | L | L | L | L | H | H | H | H | H | L | L | L | L | L | L | L | H |
| | L | L | L | L | H | H | H | H | H | H | L | L | L | L | L | L | H |
| Active LOW Output (P = H) | L | L | L | L | H | H | L | L | L | L | H | H | H | H | H | H | H |
| | L | L | L | L | H | H | L | H | L | H | H | L | H | H | H | H | H |
| | L | L | L | L | H | H | L | H | H | H | H | H | L | H | H | H | H |
| | L | L | L | L | H | H | H | L | L | H | H | H | H | L | H | H | H |
| | L | L | L | L | H | H | H | L | H | H | H | H | H | H | L | H | H |
| | L | L | L | L | H | H | H | H | L | H | H | H | H | H | H | L | H |
| | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | L | H |
| | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

| | |
|------------------------------------------------------------------------|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

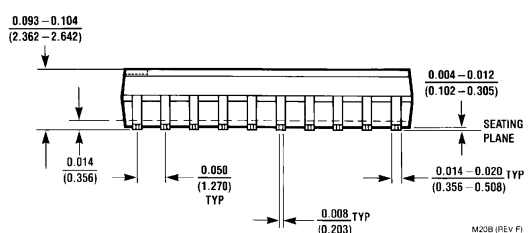
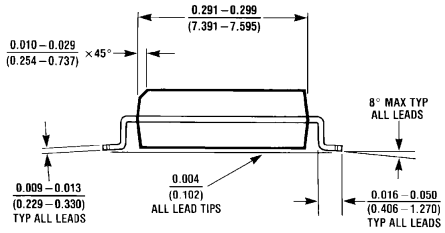
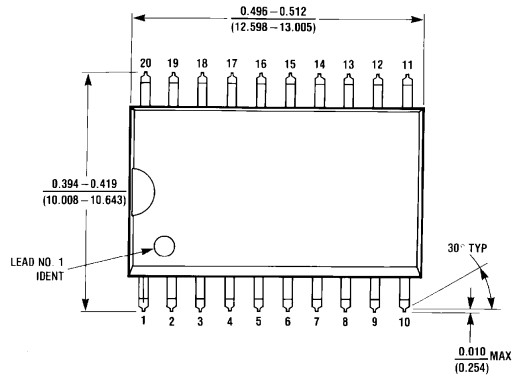
DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|---------------------|-----|-------------------------|-------|-----------------|------------------------------------------------------|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} | 2.5 | | V | Min | I _{OH} = -1 mA |
| | | 10% V _{CC} | 2.4 | I _{OH} = -3 mA | | | |
| | | 5% V _{CC} | 2.7 | I _{OH} = -1 mA | | | |
| | | 5% V _{CC} | 2.7 | I _{OH} = -3 mA | | | |
| V _{OL} | Output LOW Voltage | | | 0.5 | V | Min | I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | | 31 | 45 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | 37 | 56 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | | 37 | 56 | mA | Max | V _O = HIGH Z |

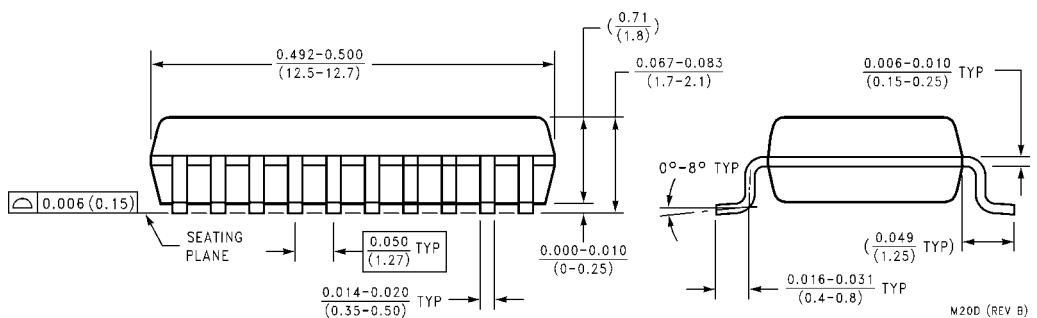
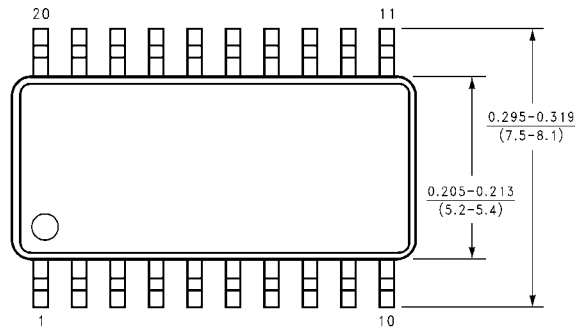
AC Electrical Characteristics

| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
|------------------|----------------------------------------------------------|-----------------------------------------------------------------------------|------|------|------------------------------------------------------------------------------------|------|-------|
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 6.0 | 11.0 | 16.0 | 6.0 | 17.0 | ns |
| t _{PHL} | A _n to O _n | 4.0 | 7.5 | 11.0 | 4.0 | 12.0 | |
| t _{PLH} | Propagation Delay | 5.0 | 8.5 | 15.0 | 5.0 | 16.0 | ns |
| t _{PHL} | \overline{E}_1 or \overline{E}_2 to O _n | 4.0 | 6.5 | 9.0 | 4.0 | 10.0 | |
| t _{PLH} | Propagation Delay | 6.0 | 11.0 | 16.0 | 6.0 | 17.0 | ns |
| t _{PHL} | E ₃ or E ₄ to O _n | 5.0 | 10.0 | 14.0 | 5.0 | 15.0 | |
| t _{PLH} | Propagation Delay | 6.0 | 11.5 | 18.0 | 6.0 | 20.0 | ns |
| t _{PHL} | P to O _n | 6.0 | 11.0 | 16.0 | 6.0 | 17.0 | |
| t _{PZH} | Output Enable Time | 3.0 | 5.5 | 10.0 | 3.0 | 11.0 | ns |
| t _{PZL} | \overline{OE}_1 or \overline{OE}_2 to O _n | 5.0 | 9.0 | 13.0 | 5.0 | 14.0 | |
| t _{PHZ} | Output Disable Time | 2.0 | 4.0 | 6.0 | 2.0 | 7.0 | |
| t _{PLZ} | \overline{OE}_1 or \overline{OE}_2 to O _n | 3.0 | 5.0 | 8.0 | 3.0 | 9.0 | |

Physical Dimensions inches (millimeters) unless otherwise noted

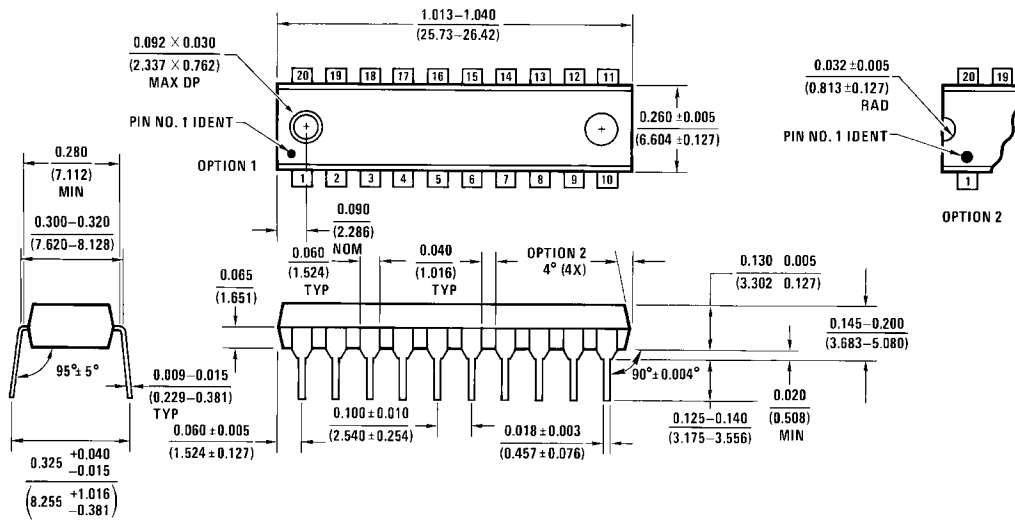


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

N20A (REV G)

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