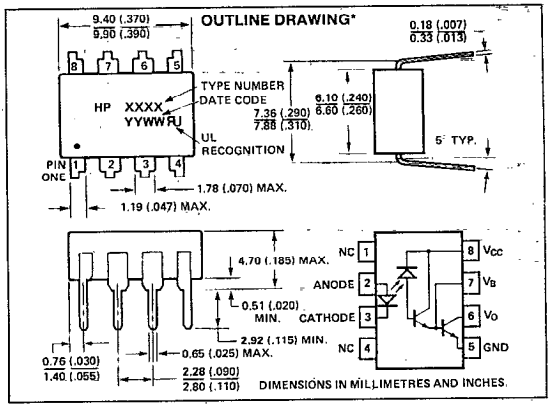
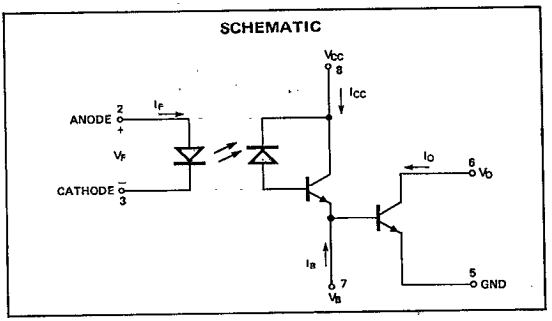
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139





Features

- **HIGH CURRENT TRANSFER RATIO — 2000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0°C TO 70°C**
  BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- **HIGH OUTPUT CURRENT — 60 mA**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 Vac, 1 MINUTE (OPTION 020)**
- **CSA APPROVED**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5700/1)**

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photo detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The 6N138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input current down to 250 μA is available upon request.

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver – Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Absolute Maximum Ratings*

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current — I_F ..... 20 mA
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage — V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current — I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 ..... -0.5 to 7 V
6N139 ..... -0.5 to 18 V
Output Power Dissipation ..... 100 mW

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.
**0° to 70° on JEDEC Registration.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 7.)

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	6N139	400* 500*	2000 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2, 4
		6N138	300*	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	2
		6N138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	6N139		0.05	100	μA	I_F = 0 mA, V_O = V_{CC} = 18 V		2, 4
		6N138		0.1	250	μA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		2
Logic High Supply Current	I_{CCH}			0.01	10	μA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		2
Input Forward Voltage	V_F			1.4	1.7* 1.75	V	T_A = 25°C, I_F = 1.6 mA	4	
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 μA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 8
Option 020	V_{ISO}		5000						
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	6N139		5	25*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					30				
				0.2	1*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					2				
		6N138		1.6	10*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					15				
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139		18	60*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					90				
				2	7*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					10				
		6N138		10	35*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10,000		V/μs	I_F = 0 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10,000		V/μs	I_F = 1.6 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6

*JEDEC registered data.
**All typicals at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

1. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device. Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ. For more information, please contact your local HP Components representative.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse. V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. $V_O < 0.8$ V).
6. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from desctructively high surge currents. The recommended value is $R_{CC} = 220\ \Omega$.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

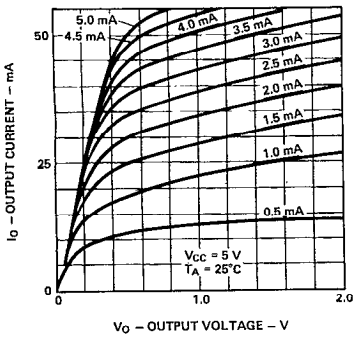


Figure 1. 6N138/6N139 DC Transfer Characteristics

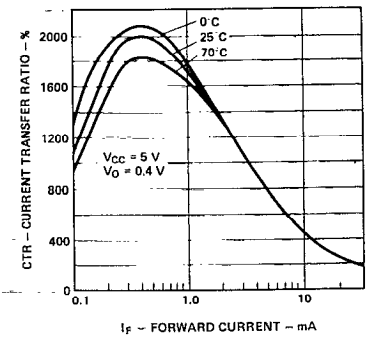


Figure 2. Current Transfer Ratio vs Forward Current 6N138/6N139

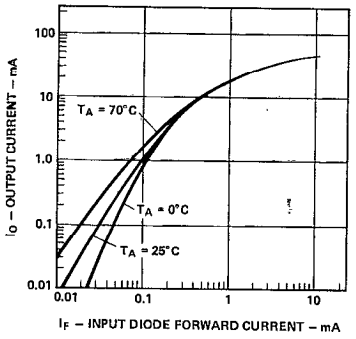


Figure 3. 6N138/6N139 Output Current vs Input Diode Forward Current

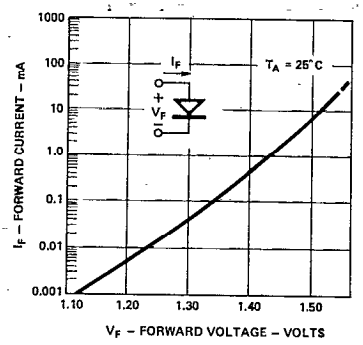


Figure 4. Input Diode Forward Current vs. Forward Voltage.

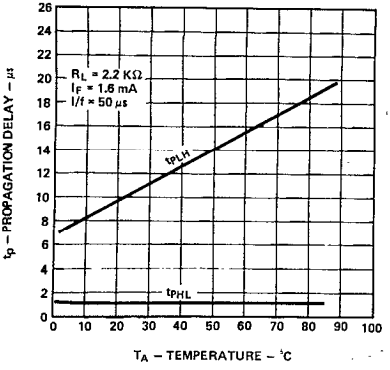


Figure 5. Propagation Delay vs. Temperature.

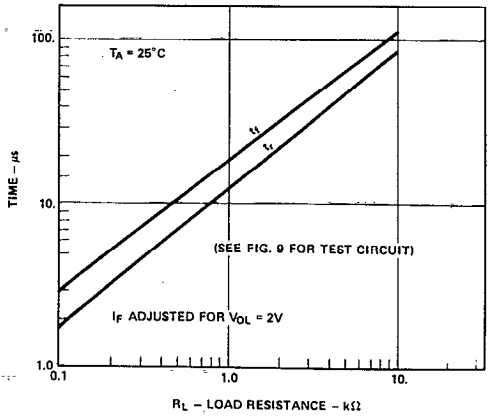


Figure 6. Non Saturated Rise and Fall Times vs. Load Resistance.

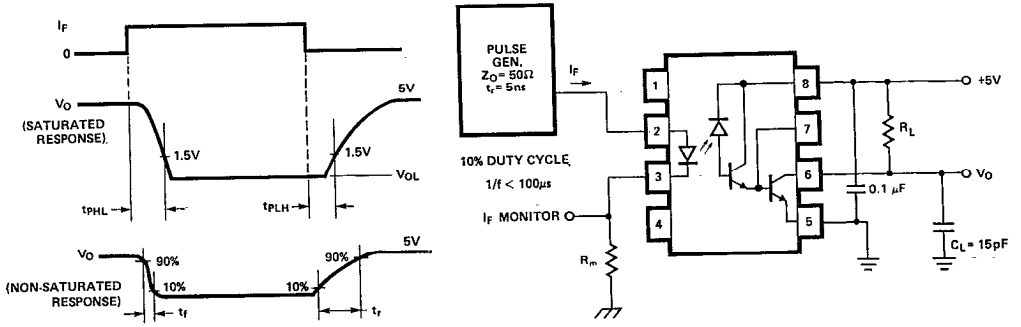


Figure 7. Switching Test Circuit.*

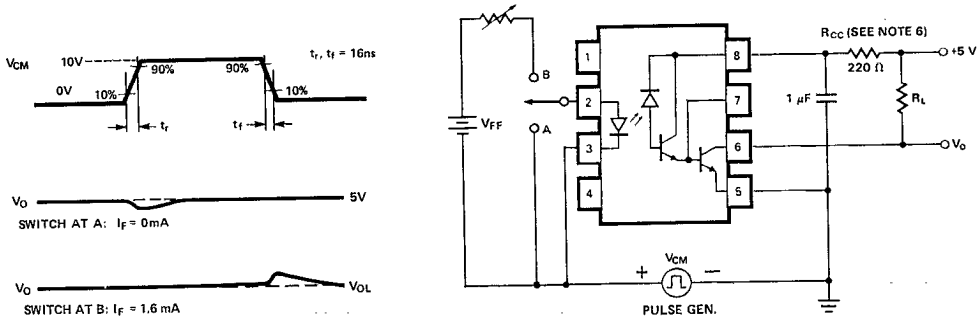


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.