

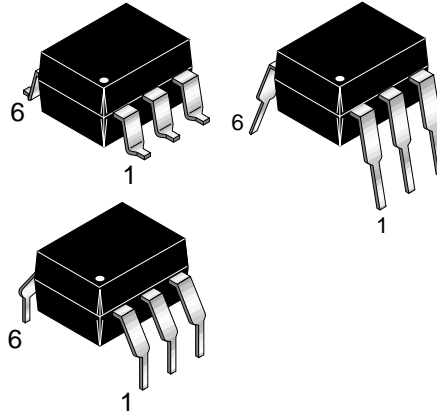
DESCRIPTION

The 4N39 and 4N40 have a gallium-arsenide infrared emitting diode optically coupled with a light activated silicon controlled rectifier in a dual in-line package.

4N39 4N40

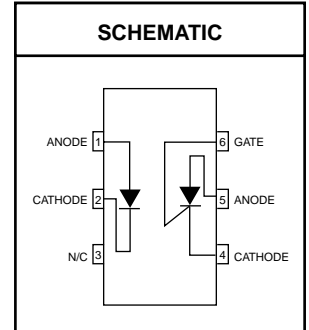
FEATURES

- 10 A, T²L compatible, solid state relay
- 25 W logic indicator lamp driver
- 400 V symmetrical transistor coupler
- Underwriters Laboratory (UL) recognized — File #E90700



APPLICATIONS

- Low power logic circuits
- Telecommunications equipment
- Portable electronics
- Solid state relays
- Interfacing coupling systems of different potentials and impedances.



Parameter	Symbol	Device	Value	Units
TOTAL DEVICE				
*Storage Temperature	T _{STG}	All	-55 to +150	°C
*Operating Temperature	T _{OPR}	All	-55 to +100	°C
*Lead Solder Temperature	T _{SOL}	All	260 for 10 sec	°C
*Total Device Power Dissipation (-55°C to 50 °C) Derate above 50°C	P _D	All	450	mW
			9.0	mW/°C
EMITTER				
*Continuous Forward Current	I _F	All	60	mA
*Reverse Voltage	V _R	All	6	V
*Forward Current - Peak (300 μs, 2% Duty Cycle)	I _{F(pk)}	All	1.0	A
*LED Power Dissipation (-55°C to 50 °C) Derate above 50°C	P _D	All	100	mW
			2.0	mW/°C
DETECTOR				
*Off-State And Reverse Voltage		4N39	200	V
		4N40	400	V
*Peak Reverse Gate Voltage			6	V
*Direct On-State Current			300	mA
*Surge On-State Current (100 μs)			10	A
*Peak Gate Current			10	mA
*Detector Power Dissipation (-55°C to 50°C) Derate above 50°C	P _D	All	400	mW
			8.0	mW/°C

Note

* Indicates JEDEC Registered Data

** Typical values at T_A = 25°C

4N39	4N40
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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
Input Forward Voltage	$I_F = 10\text{ mA}$	V_F	All		1.1	1.5	V
Reverse Leakage Current	$V_R = 3\text{ V}$	I_R	All			10	μA
Capacitance	$V_F = 0\text{ V}, f = 1.0\text{ MHz}$	C_J	All		50		pF
DETECTOR							
Peak Off-State Voltage	$R_{GK} = 10\text{ k}\Omega, T_A = 100^\circ\text{C}$	V_{DM}	4N39	200			V
			4N40	400			
Peak Reverse Voltage	$T_A = 100^\circ\text{C}$	V_{RM}	4N39	200			V
			4N40	400			
On-State Voltage	$I_T = 300\text{ mA}$	V_T	All			1.3	V
Off-State Current	$V_{DM} = 200\text{ V}, T_A = 100^\circ\text{C},$ $I_F = 0\text{ mA}, R_{GK} = 10\text{ k}\Omega$	I_{DM}	4N39			50	μA
			4N40			150	
Reverse Current	$V_R = 200\text{ V}, T_A = 100^\circ\text{C}, I_F = 0\text{ mA}$	I_R	4N39			50	μA
			4N40			150	
Holding Current	$V_{FX} = 50\text{ V}, R_{GK} = 27\text{ k}\Omega$	I_H	All			1.0	mA

TRANSFER CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Device	Min	Typ**	Max	Units
*Input Current to Trigger	$V_{AK} = 50\text{ V}, R_{GK} = 10\text{ k}\Omega$	I_{FT}	4N39			30	mA
	$V_{AK} = 100\text{ V}, R_{GK} = 27\text{ k}\Omega$		4N40			14	
*Turn-On Time	$V_{AK} = 50\text{ V}, I_F = 30\text{ mA}$ $R_{GK} = 10\text{ k}\Omega, R_L = 200\ \Omega$	t_{on}	ALL			50	μA
Package Capacitance (input to output)	$f = 1\text{ MHz}$ Input to Output Voltage = 0	C_{I-O}	ALL			2	pF
Coupled dv/dt, input to output (figure 13)		dV/dt	ALL	500			V/ μS

ISOLATION CHARACTERISTICS

Characteristic	Test Conditions	Symbol	Min	Typ**	Max	Units
*Input-Output Isolation Voltage	($I_{I-O} \leq 1\ \mu\text{A}, V_{rms}, t = 1\text{ min.}$)	V_{ISO}	5300			Vac(rms)
*Isolation Resistance	($V_{I-O} = 500\text{ VDC}$)	R_{ISO}	10^{11}			Ω
Isolation Capacitance	($V_{I-O} = \emptyset, f = 1\text{ MHz}$)	C_{ISO}		0.8		pf

Note

* Indicates JEDEC Registered Data

 ** Typical values at $T_A = 25^\circ\text{C}$

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Figure 1. Input Current To Trigger vs. Anode-Cathode Voltage

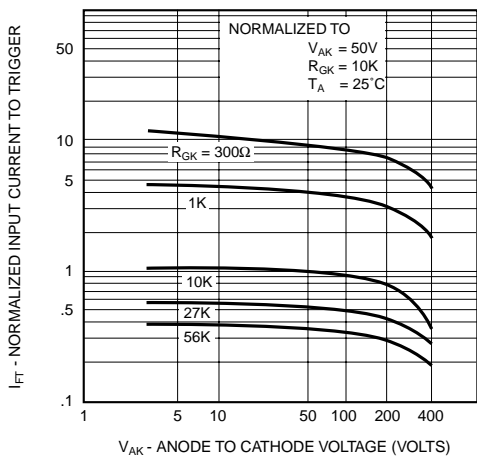


Figure 2. Input Current To Trigger vs. Temperature

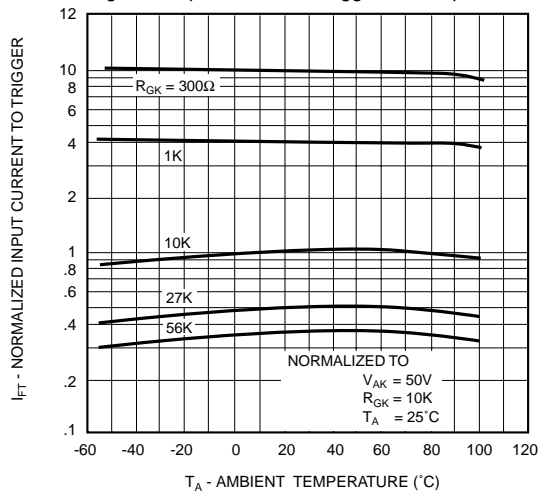


Figure 3. Input Current To Trigger Distribution vs. Temperature

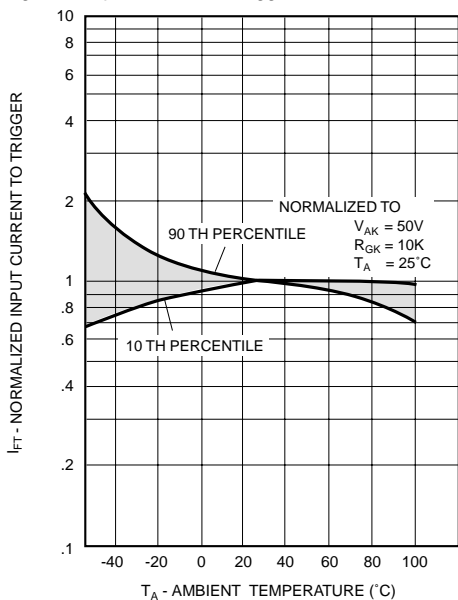


Figure 4. Input Current To Trigger vs. Pluse Width

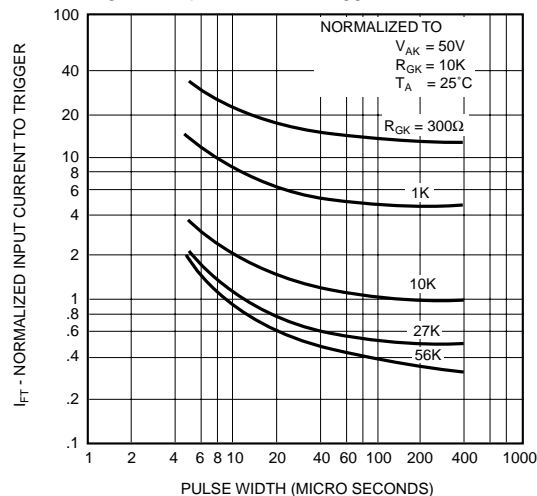


Figure 5. Turn-On Time vs. Input Current

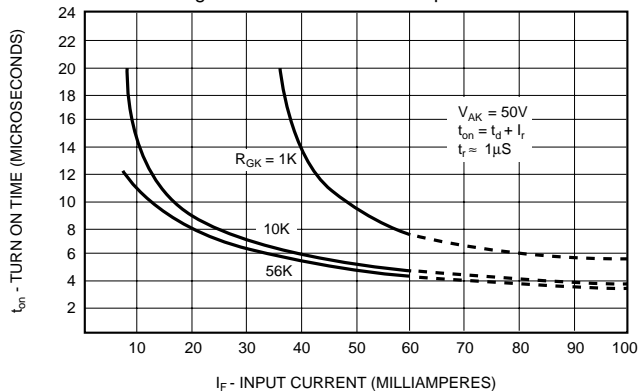
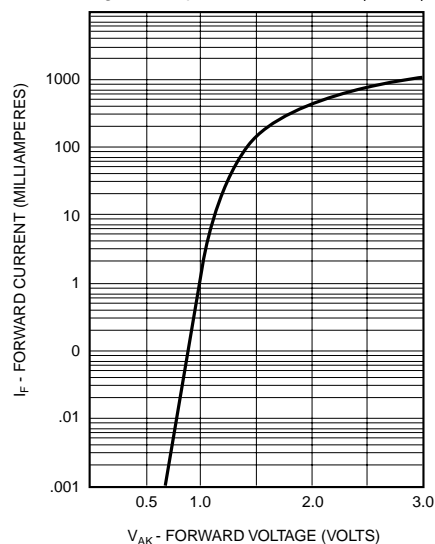


Figure 6. Input Characteristics I_F vs. V_F



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Figure 7. Holding Current vs. Temperature

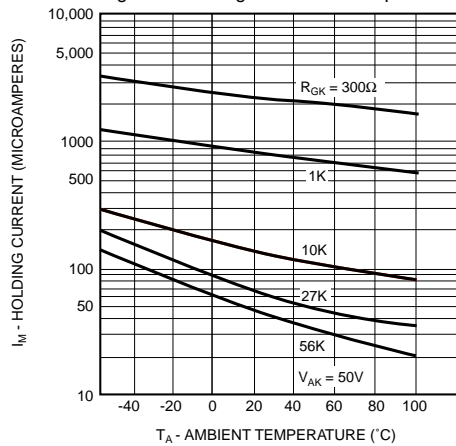


Figure 8. Maximum Transient Thermal Impedance

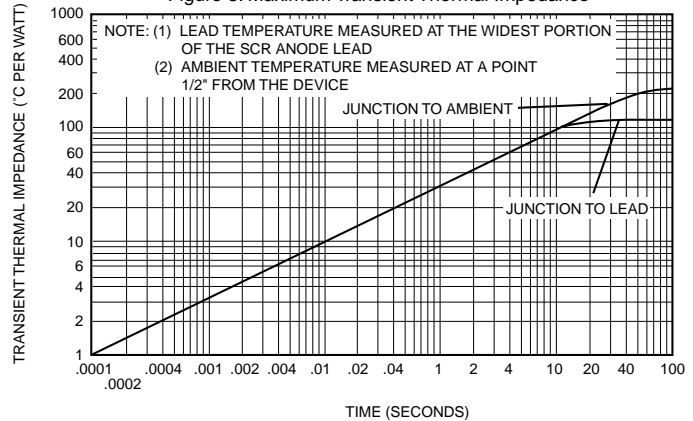


Figure 9. Off-State Forward Current vs. Temperature

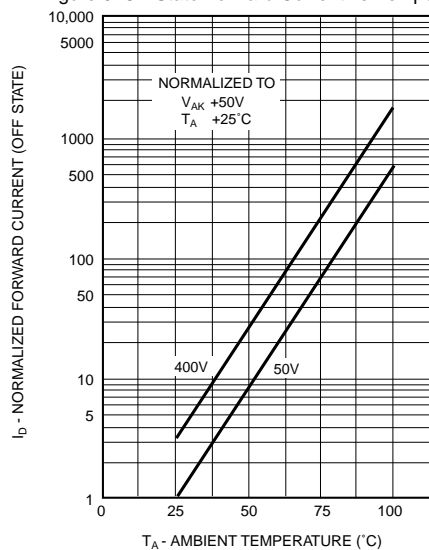


Figure 10. On-State Current vs. Maximum Allowable Temperature

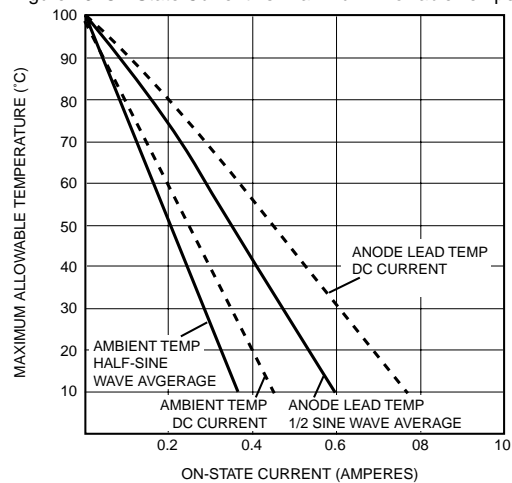


Figure 11. dv/dt vs. Temperature

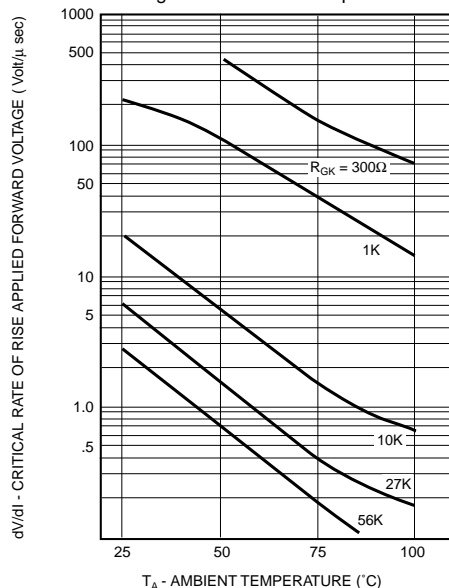
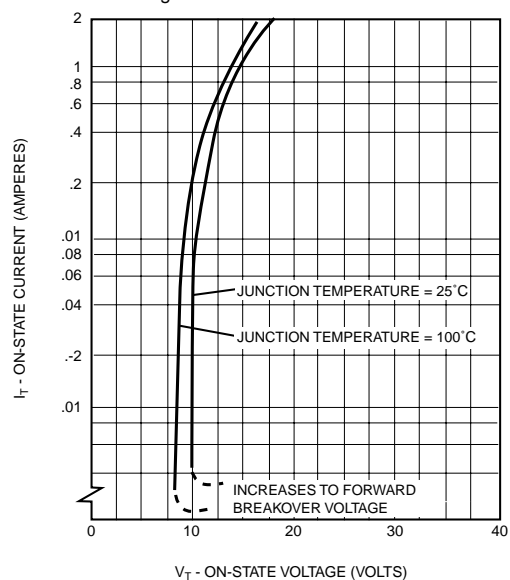


Figure 12. On-State Characteristics



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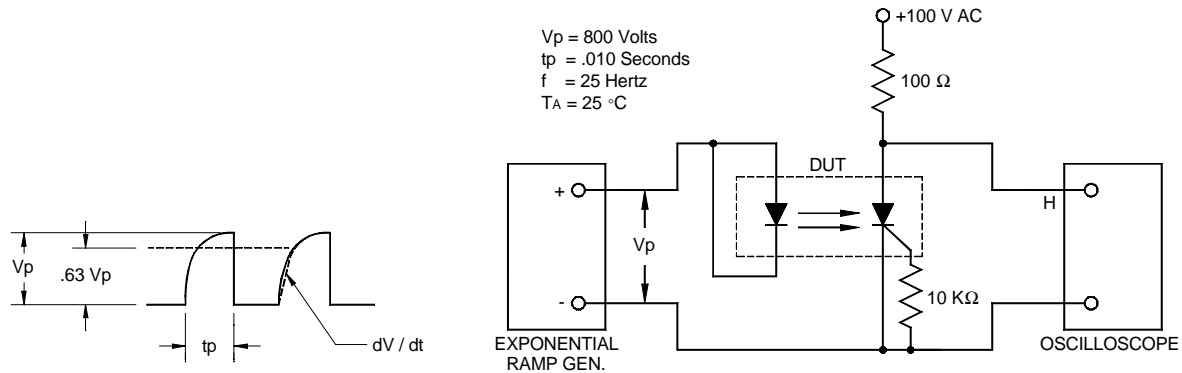
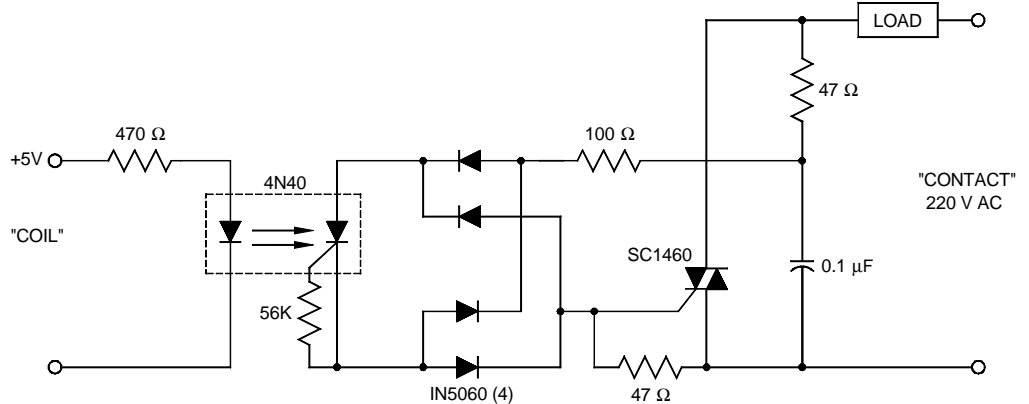


Fig. 13 Coupled dv/dt - Test Circuit

TYPICAL APPLICATIONS

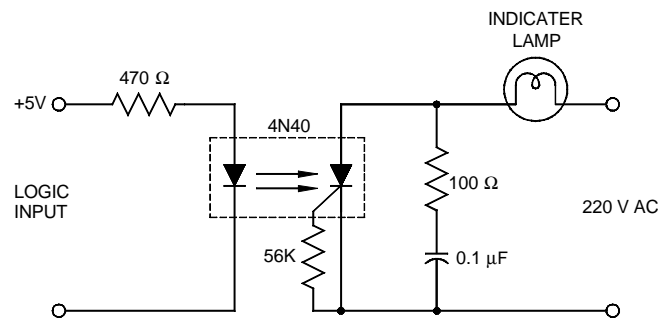
10A, T²L COMPATIBLE, SOLID STATE RELAY

Use of the 4N40 for high sensitivity, 5300 V isolation capability, provides this highly reliable solid state relay design. This design is compatible with 74, 74S and 74H series T²L logic systems inputs and 220V AC loads up to 10A.



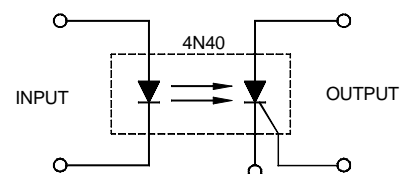
25W, LOGIC INDICATOR LAMP DRIVER

The high surge capability and non-reactive input characteristics of the 4N40 allow it to directly couple, without buffers, T²L and DTL logic to indicator alarm devices, without danger of introducing noise and logic glitches.



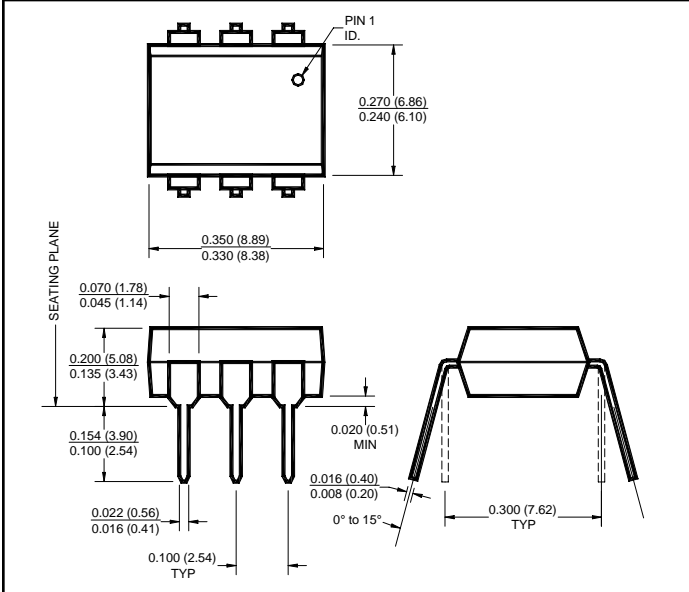
400V SYMMETRICAL TRANSISTOR COUPLER

Use of the high voltage PNP portion of the 4N40 provides a 400V transistor capable of conducting positive and negative signals with current transfer ratios of over 1%. This function is useful in remote instrumentation, high voltage power supplies and test equipment. Care should be taken not to exceed the 40mW power dissipation rating when used at high voltages.

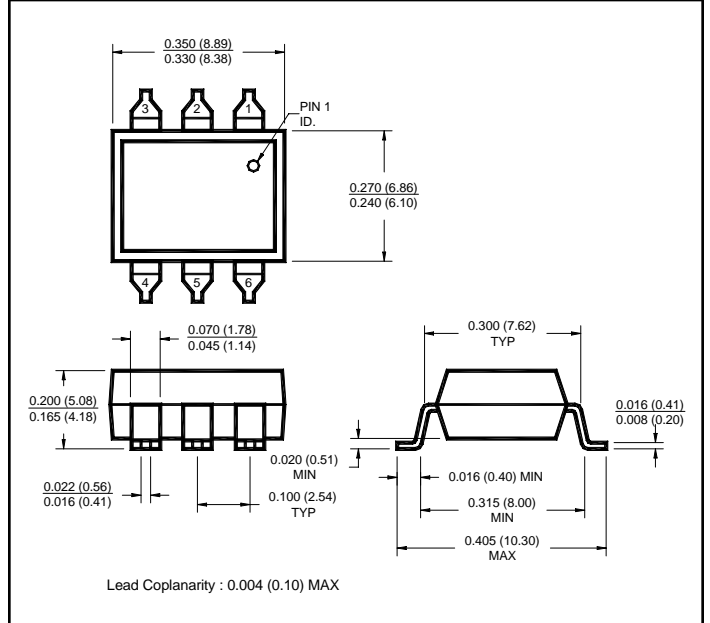


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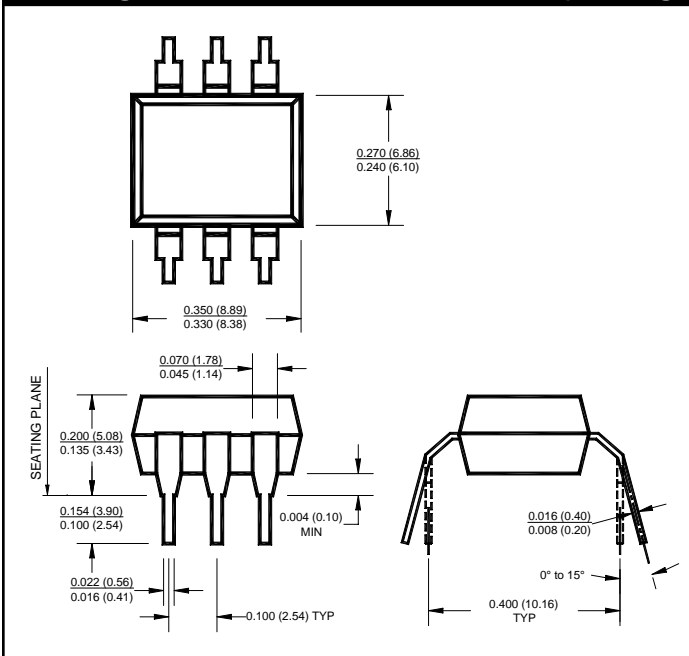
Package Dimensions (Through Hole)



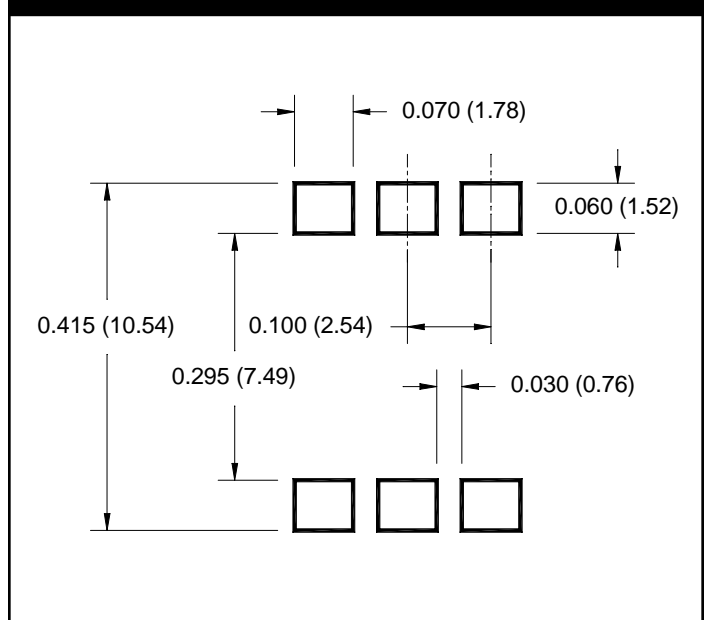
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



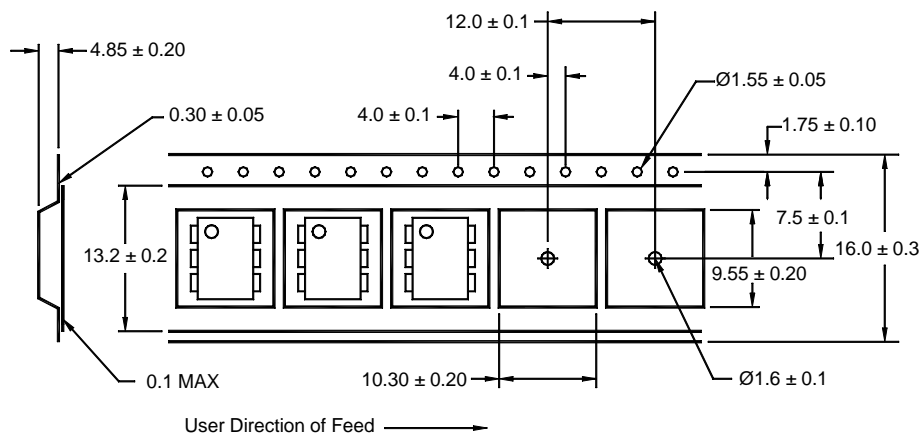
NOTE

All dimensions are in inches (millimeters)

ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing
300	.300	VDE 0884
300W	.300W	VDE 0884, 0.4" Lead Spacing
3S	.3S	VDE 0884, Surface Mount
3SD	.3SD	VDE 0884, Surface Mount, Tape & Reel

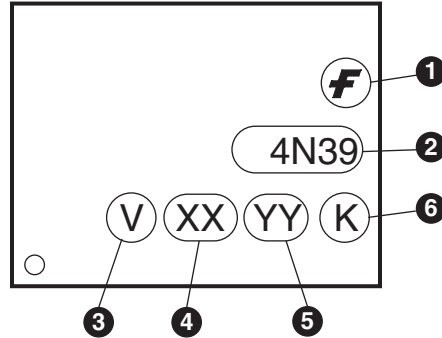
Carrier Tape Specifications ("D" Taping Orientation)



NOTE

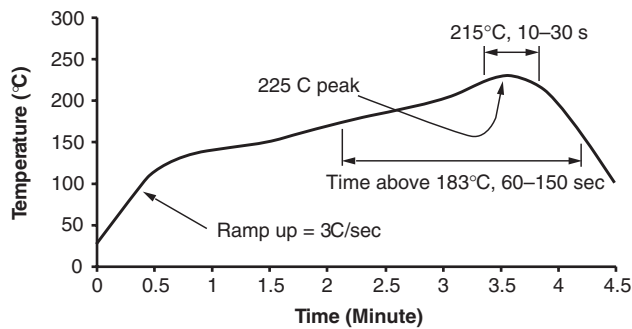
All dimensions are millimeters

MARKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Reflow Profile (Black Package, No Suffix)



- Peak reflow temperature: 225°C (package surface temperature)
- Time of temperature higher than 183°C for 60-150 seconds
- One time soldering reflow is recommended

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E ² CMOS™	μC™	MSXPro™	Quiet Series™	TINYOPTO™
EnSigna™	i-Lo™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	μSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	VCX™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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