Philips Components-Signetics

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Memory Products	

27C040

4 MEG CMOS EPROM (512K × 8)

DESCRIPTION

The 27C040 CMOS EPROM is a 4,194,304 bit 5V read only memory organized as 524,288 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high performance speeds, and immunity from noise. The 27C040 has non-multiplexed addressing interface.

The 27C040 is available in a ceramic windowed DIP and a plastic DIP.

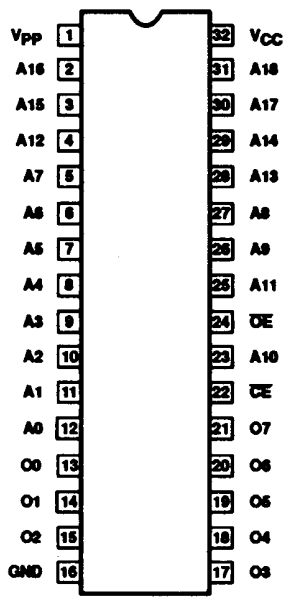
The 27C040 can be programmed on industry standard EPROM programmers, using the intelligent algorithm or quick pulse programming techniques.

FEATURES

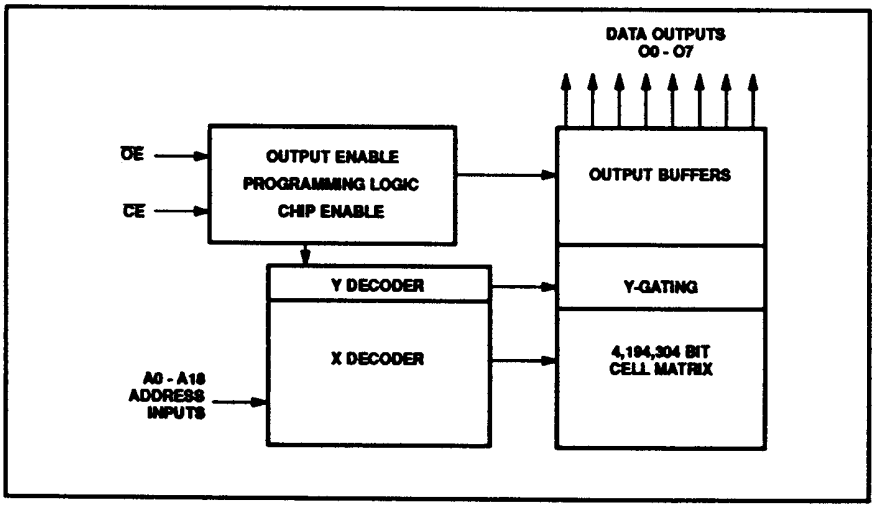
- Low power consumption
  - 100μA standby current
- Quick pulse programming algorithm for high speed production programming
- High-performance speed
  - 150ns maximum access time
- Noise immunity features:
  - ±10% V_{CC} tolerance
  - Maximum latch-up immunity through Epitaxial processing

PIN CONFIGURATIONS

FA, N Packages



BLOCK DIAGRAM



PIN DESCRIPTION

A0 - A18	Address
O0 - O7	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't Use

4 MEG CMOS EPROM (512K × 8) 27C040

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
32-Pin Ceramic Dual In-Line with quartz window	27C040-15 FA
32-Pin Ceramic Dual In-Line with quartz window	27C040-20 FA
32-Pin Plastic Dual In-Line	27C040-15 N
32-Pin Plastic Dual In-Line	27C040-20 N

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
T_{stg}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-0.6 to (V_{CC} + 1)	V
V_H	Voltage on A_9 (during intelligent identifier interrogation)	-0.6 to +13.0	V
V_{PP}	Voltage on V_{PP} pin (during programming)	-0.6 to +14.0	V
V_{CC}	Supply voltage	-0.6 to +7.0	V

NOTES:
1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

OPERATING TEMPERATURE RANGE

PARAMETER	RATING (°C)
Operating temperature range: T_{amb}	COMMERCIAL 0 to +70

4 MEG CMOS EPROM (512K × 8) 27C040

DEVICE OPERATION[1]

MODE		$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[2]	X	V_{CC}	5.0V	D_{OUT}
Output disable		V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	Hi-Z
Standby		V_{IH}	X	X	X	V_{CC}	5.0V	Hi-Z
Programming		V_{IL}	V_{IH}	X	X	V_{PP}[5]	V_{CC}[5]	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}[5]	V_{CC}[5]	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	V_{PP}[5]	V_{CC}[5]	Hi-Z
Intelligent	Manufacturer[4]	V_{IL}	V_{IL}	V_H[3]	V_{IL}	V_{CC}	5.0V	F5 (HEX)
Identifier	Device[4]	V_{IL}	V_{IL}	V_H[3]	V_{IH}	V_{CC}	5.0V	3E (HEX)

NOTES:
1. All voltages are with respect to network ground.
2. X can be V_{IL} or V_{IH}.
3. $V_H = 12.0V \pm 0.5V$, $V_{CC} = 5.0V \pm 0.5V$.
4. A1 - A8, A10 - A18 = V_{IL}.
5. See DC Programming Characteristics for V_{CC} and V_{PP} voltages.

READ MODE: 27C040

The 27C040 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE:

The 27C040 can be placed in the standby mode which reduces the maximum I_{CC} of the device by applying a V_{IH} to the $\overline{CE}$ pin. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT "OR-TIEING" 2 LINE OUTPUT CONTROL:

The 27C040 may be used in larger memory systems. A two line control function has been provided to allow for:

- The lowest possible memory power consumptions and,
- Complete assurance that bus contention will not occur.

To use this feature, $\overline{CE}$ should be decoded and used as the primary device selecting function, and $\overline{OE}$ should be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS:

During the switch between active and standby power conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk eletrolytic capacitor should be used between V_{CC} and GND for every eight (8) devices. The location of the capacitor should be close to where the power supply is connected to the array.

DC ELECTRICAL CHARACTERISTICS

Over operating temperature range, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[3]	MAX	
Input current						
I_{IH}	Leakage High	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Leakage Low	$V_{IL} = 0V$		0.01	-1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			10	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$, $V_{OUT} = 5.5V = V_{CC}$	-10.0		10.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4, 6]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$, O0 - 15 = 0mA			50	mA
I_{CC} CMOS	Operating (CMOS inputs)[4, 6]	$\overline{CE}$ = GND, f = 6.7MHz Inputs = V_{CC} or GND, I/O = 0mA			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1	mA
I_{SB} CMOS	Standby (CMOS inputs)[5]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-.02		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_{amb} = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$, f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$, $V_{OUT} = 0V$			12	pF

NOTES:

1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_{amb} = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 6.7MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

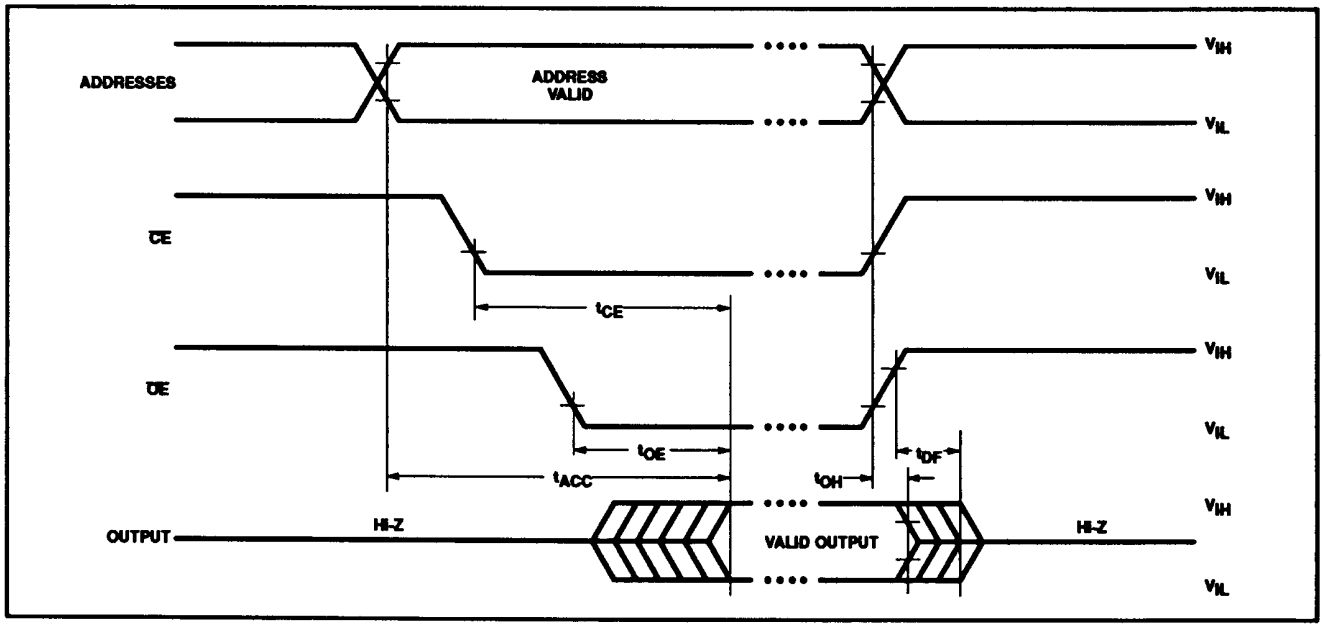
Over operating temperature range, +4.5V ≤ V_{CC} ≤ +5.5V, R_L = 660Ω, C_L = 100pF

SYMBOL	TO	FROM	LIMITS				UNIT
			27C040-15		27C040-20		
			MIN	MAX	MIN	MAX	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		60		70	ns
Disable time[2]							
t_{DF}	Output Hi-Z	$\overline{OE}$		50		60	ns
t_{OH}	Output Hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

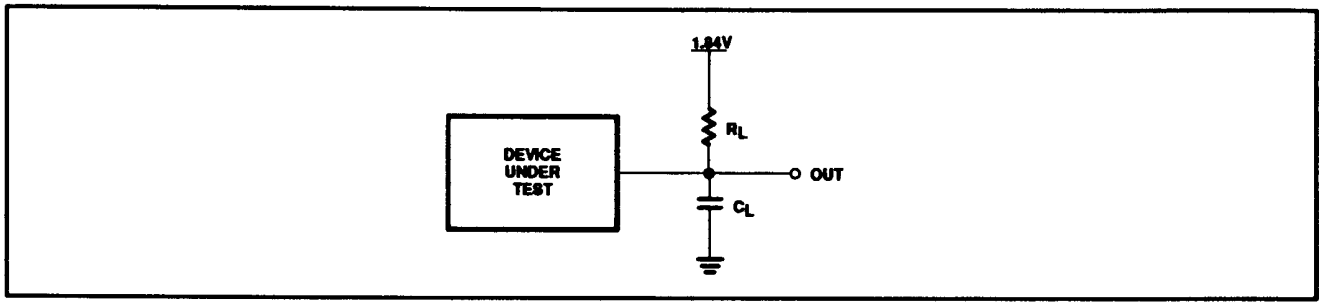
NOTES:

1. AC characteristics are tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V; Input rise and fall times (10% to 90%) = 20ns.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT



PROGRAMMING INFORMATION

Complete programming system specifications for both the intelligent programming method and for the quick-pulse programming method are available upon request from Signetics.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of 27C040 programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Memory Marketing.

PROGRAMMING THE 27C040

Caution: Exceeding 14.0V on V_{PP} pin may permanently damage the 27C040.

Initially, all bits of the 27C040 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

QUICK-PULSE PROGRAMMING ALGORITHM

Signetics plastic EPROMs can be programmed using the quick-pulse programming algorithm to substantially reduce the throughput time in the production environment. This algorithm typically allows plastic devices to be programmed in under twelve seconds, a significant improvement over previous algorithms. Actual programming time is a function of the PROM programming equipment being used.

The quick-pulse programming algorithm uses initial pulses of 100µs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100µs pulses per byte are provided before a failure is recognized (refer to the following pages for algorithm specifications).

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C040 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C040 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C040 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C040 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The 27C040 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C040 can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C040 intelligent programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Actual programming times may vary due to differences in programming equipment.

The intelligent identifier also provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25° ± 5°C ambient temperature range that is required when programming the 27C040. To activate this mode, the programming equipment must force 11.5V to 12.5V on address A9 of the 27C040. Two bytes may then be read from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. The $\overline{CE}$, $\overline{OE}$ and all other address lines must be at V_{IL} during interrogation.

The identifier information for Signetics 27C040 is as follows:

When A0 = V_{IL}	
data is "Manufacturer"	$15_{(HEX)}$
When A0 = V_{IH}	
data is "Product"	$3E_{(HEX)}$

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. The programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which is then followed by a longer overprogram pulse of 3Xms. X is an iteration counter and is equal to the number of the initial 1ms pulses applied to a particular location before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram pulse is applied (refer to the following pages for algorithm specifications).

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features that add to system reliability. These include input/output protection to latch-up for stresses up to 100mA on Address and Data pins that range from -1V to (V_{CC} + 1V). In addition, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Signetics warranty for programmability extends only to product that has been programmed on *certified* equipment that has been serviced to the manufacturers recommendation.

INTELLIGENT PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25°C ±5°C, V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.4	6.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O0 - 15 = 0mA		50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	Note 1	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	Note 2	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	µs

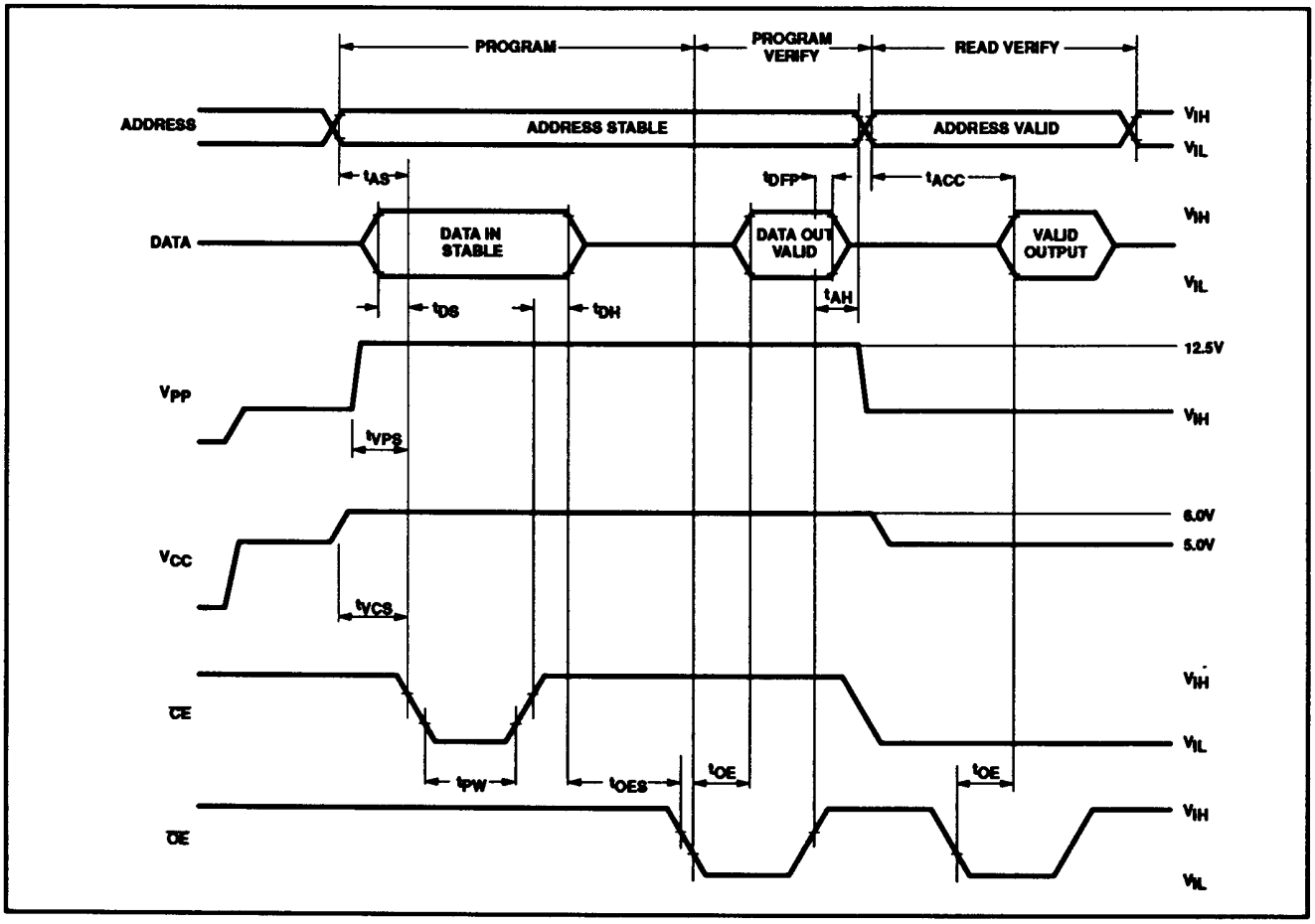
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

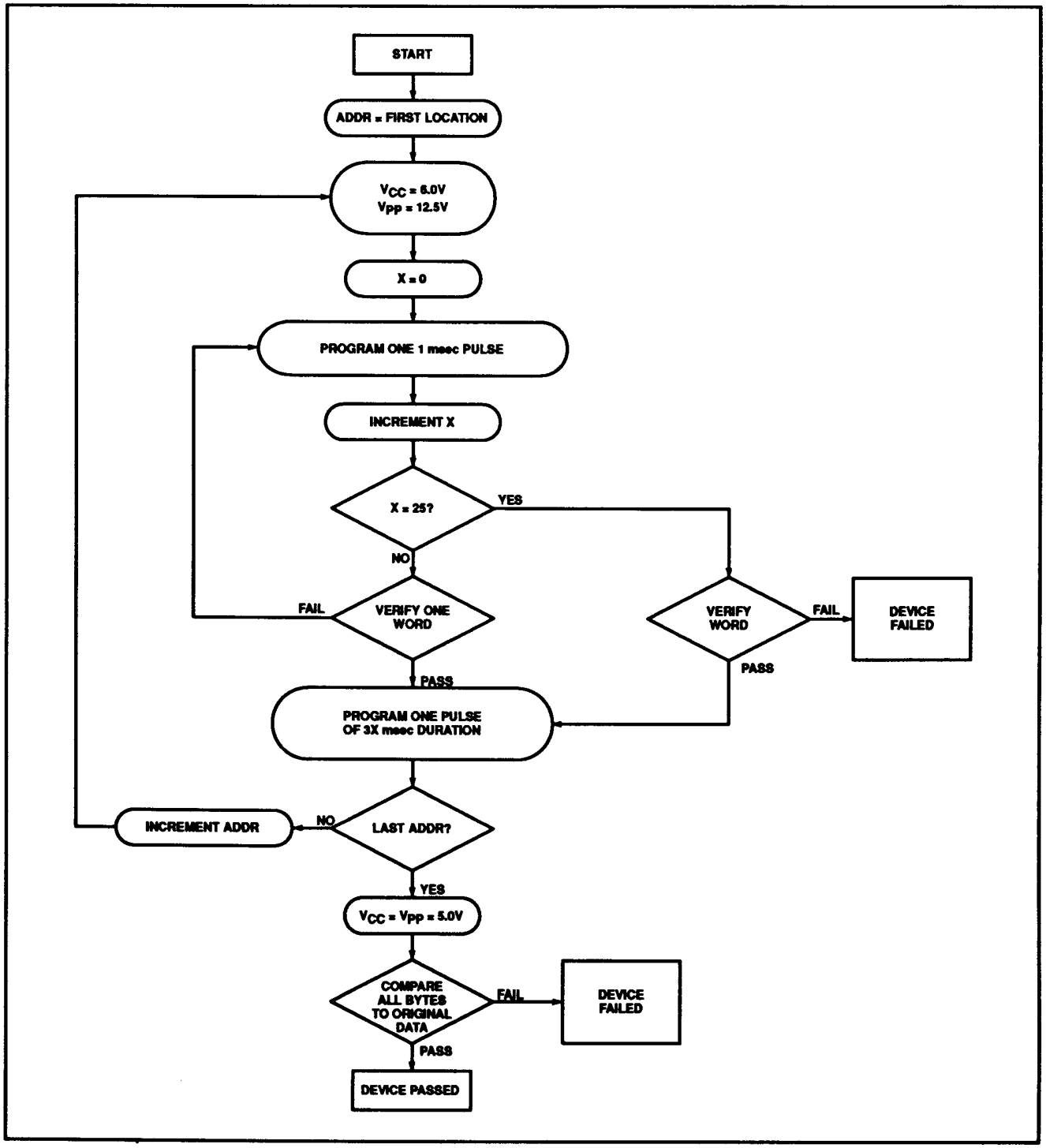
NOTES:

1. Initial program pulse width tolerance is 1ms ±5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
3. The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
4. During programming, a 0.1µf capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

INTELLIGENT PROGRAMMING ALGORITHM WAVEFORMS



INTELLIGENT PROGRAMMING ALGORITHM FLOWCHART



QUICK PULSE PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25°C ±5°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.4	6.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O0 - 15 = 0mA		50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	Note 1	.095	0.100	0.105	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	Note 2	2.85		78.8	ms
t_{OE}	Data valid from $\overline{OE}$				150	µs

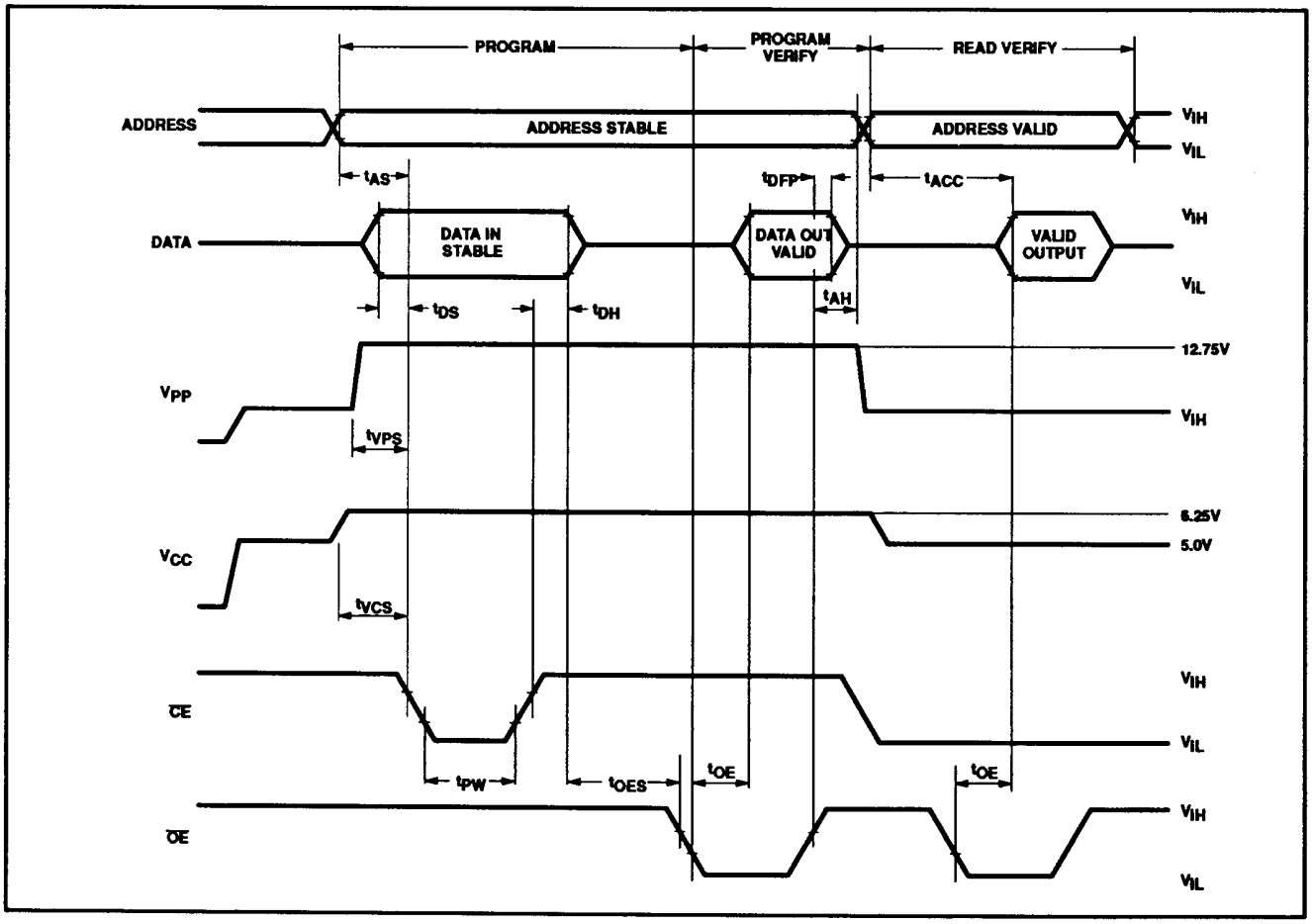
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

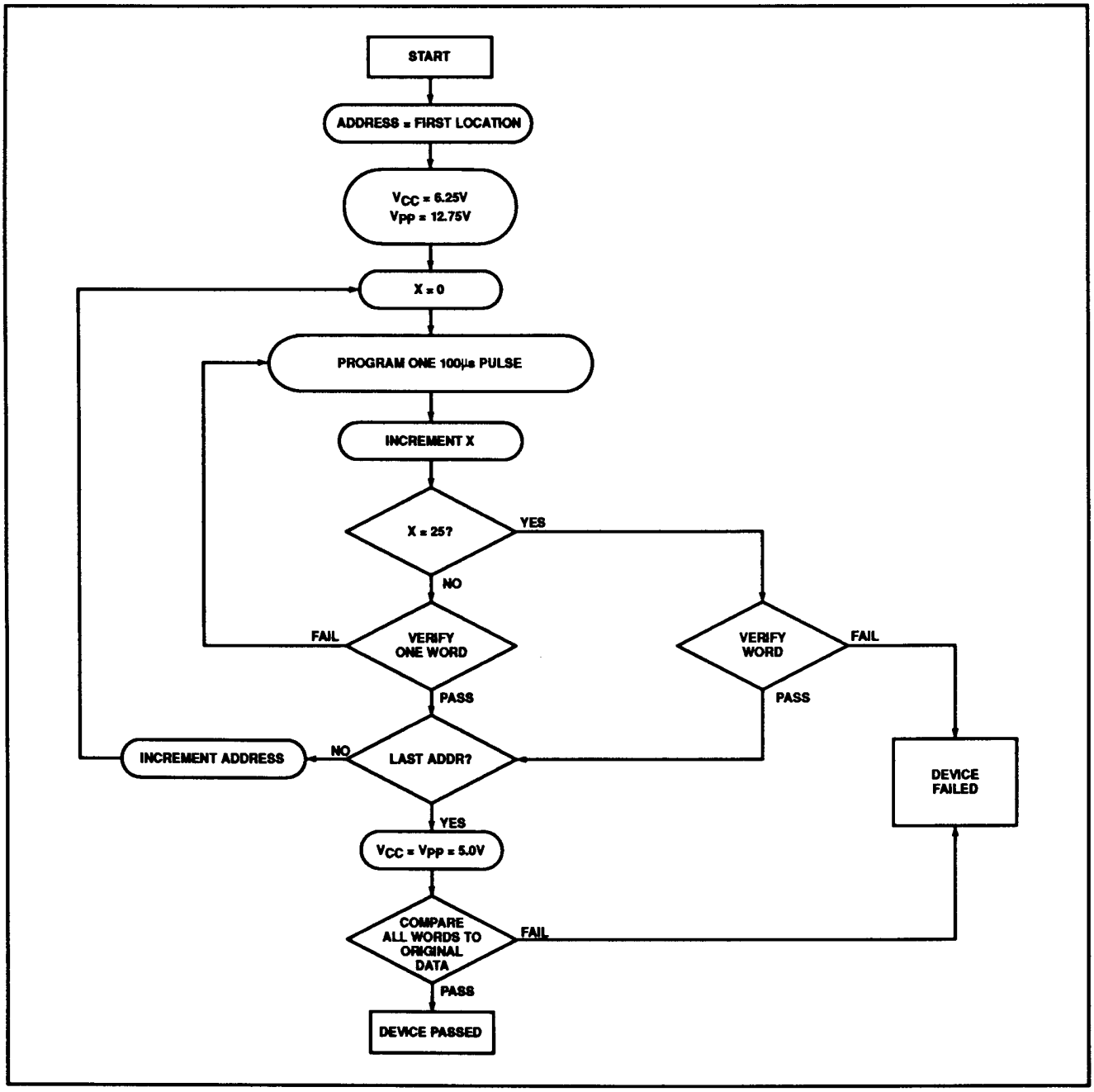
NOTES:

1. Initial program pulse width tolerance is 1ms ±5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
3. The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
4. During programming, a 0.1µf capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

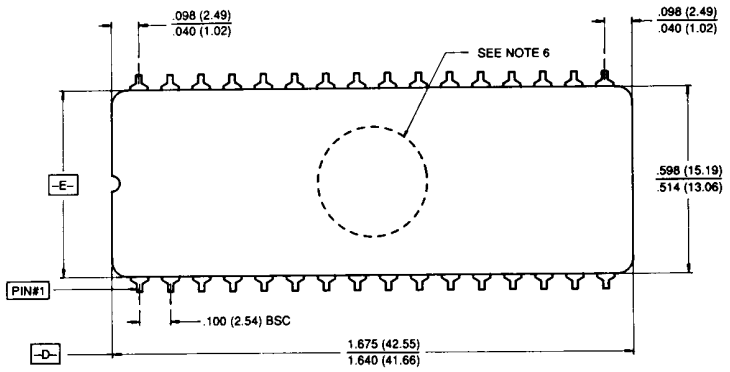
QUICK PULSE PROGRAMMING ALGORITHM WAVEFORMS

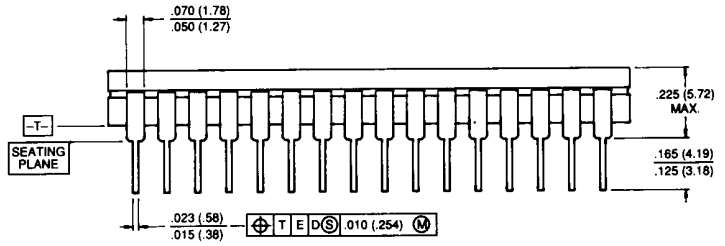


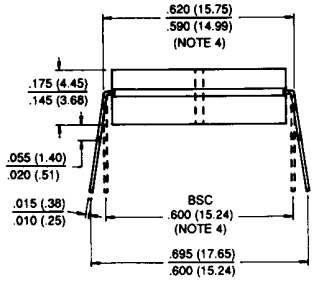
QUICK PULSE PROGRAMMING ALGORITHM FLOWCHART



32-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE







NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS ARE SHOWN IN PARENTHESIS.
2. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
3. "T", "D", AND "E" ARE REFERANCE DATUMS ON THE BODY AND INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS ON THE SEAL LINE, AND LID TO BASE MISMATCH.
4. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#32 WHEN VIEWED FROM THE TOP.
6. DENOTES WINDOW LOCATION FOR EPROM PRODUCTS.

853-1469 00351 FR3

4 MEG CMOS EPROM (512K × 8) 27C040

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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98-6232-040 0382N/4M/FP/1290